Abstract: Recently, long-term evolution (LTE) advanced has been dominated as the next-generation wireless communication standard, which is aimed at higher peak data rates close to 4 Gb/s. This is accomplished by adopting efficient channel coding schemes. Turbo codes are the best suited for FEC (Forward Error Correction) in channel coding which also has near Shannon error-correcting performance. But at the same time it is also necessary to have compactness in area, so a novel ACS (Add-Compare-Select) unit is proposed which reduces the computational area occupied in the decoder unit. The turbo decoder, which is specified in LTE, reveals to be a limiting block toward this goal due to its iterative decoding nature, high latency, and significant silicon area consumption. Since the implementation of the actual maximum a posteriori (MAP) algorithm incurs very high computational complexity, typically, two modified forms of the MAP algorithm, i.e., the max-log-MAP and log-MAP algorithms are commonly realized instead. In these two alternative methods, the MAP core consists of log-likelihood ratio (LLR) units, as well as the core units to compute \( \alpha \), \( \beta \), and \( \gamma \), i.e., the forward, backward, and branch metrics, respectively. The main aim of this project is to reduce the area occupied by computational units in decoder block by employing the ACS architecture by simplifying the computations.

Keywords: LTE, Turbo Codes, ACS unit, MAP Algorithm, MSR Architecture, LLR Units.

I. INTRODUCTION

The wireless communication technology which has connected the people all over the world from anywhere anytime is now rapidly growing on demand to achieve high data rate transmissions. To accomplish this, a reliable channel coding scheme has to be adopted. Turbo codes are one of the high performance channel codes with forward error correction (FEC) which provides optimal performance approaching the Shannon limit \[1\]. The name "turbo code" arose from the feedback loop used during normal turbo code decoding, which was analogized to the exhaust feedback used for engine turbo charging. This scheme is mainly used in the digital communication systems where the transmitted signals often get corrupted by noise due to their non-ideal behavior in realistic communication channels. So, turbo codes are used at the most in long term evolution (LTE) systems. In this paper, the architecture of turbo encoder and modified turbo decoder are proposed. The main aim is to reduce the area occupied by computational units in decoder block by employing the ACS 4 unit along with MSR (Maximum Shared Resource) architecture by simplifying the computations. Hence in this different turbo decoding algorithms which are used to increase the performance of the decoder are discussed. The proposed scheme results in, at most, an 18.1% reduction in the silicon area compared with the designs reported to date. This project was implemented by using XILINX-ISE 12.4i (Verilog HDL) and simulated using MODELSIM Altera 6.6g_p1.

II. TURBO ENCODING ARCHITECTURE

The turbo encoder consists of two identical RSC encoders as shown in Fig.1. The two encoders receive the same data, but the lower encoder receives the data after passing through an interleaver. The interleaver is a mapping device that permutes the order of symbols in deterministic manner; it takes symbols at inputs and produces identical symbols at the output but in different temporal order. Two types of interleavers are periodic and pseudo-random. Pseudo random interleavers give random permutations of block symbols, and as the size of the interleaver increases BER performance. The superior performance of Turbo codes over convolutional codes is achieved only when the length of the interleaver is very large, on the order of several thousand bits \[3\]. For large block size interleavers, most random inter-leavers perform well. On the other hand, for some applications it is preferable to have a deterministic interleaver, to reduce the hardware requirements for interleaving and de-interleaving operations. There are two major criteria in the design of an interleaver: 1) the distance spectrum properties (weight distribution) of the code, and 2) the correlation between the soft output of each decoder corresponding to its parity bits and the information input data sequence. Criterion 2 is sometimes referred to as the iterative decoding suitability (IDS) criterion \[3\].

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This is a measure of the effectiveness of the iterative decoding algorithm and the fact that if these two data sequences are less correlated, then the performance of the iterative decoding algorithm improves. An interleaver is a device that rearranges the ordering of sequence of symbols in a deterministic manner. The two main issues in the interleaver design are the interleaver size and interleaver map. Interleaving is used to feed the encoders with permutations so that the generated redundancy sequences can be assumed independent.

III. TURBO DECODING ARCHITECTURE

The turbo decoder mainly consists of serially connected soft-input soft-output (SISO) decoders with interleaver in between and the corresponding deinterleaver (it performs reverse operation of interleaver). Deinterleaver performs the reverse operation of interleaver. These are designed and used in the context of characteristics of the errors that might occurs when the message bits are transmitted through a noisy channel. To understand the functions of a deinterleaver, understanding of error characteristics is essential. The outputs of encoded unit serve as input to the decoder unit. Thus the decoder has three inputs and which on iterative decoding produces the output Dk. The decoders considered here are MAP (Maximum A Posteriori) decoders. The block representation is shown in fig-2.

The MAP decoder1 receives the systematic and parity1 data bits, which on decoding produces a soft value which is an extrinsic estimate, these values are interleaved and again laid as input to MAP decoder 2. After decoding, again the output is sent into the deinterleaver, thus it now consists of second estimated extrinsic values which intern is again feedback into the MAP decoder1. There is continuous iterations taking place between MAP decoder1 and 2 units until the error rate is found to be null in the last stage simple approximations are performed to obtain the hard decision values at the MAP decoder2 stage.

A. Turbo Decoder Algorithms

In 1974, Bahl, Cocke, Jelinek and Raviv proposed the posteriori probabilities based decoding algorithm which later came to be known as MAP algorithm. There are other schemes of MAP algorithm which makes the computations easier and faster, they are; log-MAP and Max-log-MAP algorithm. The MAP decoders receive the input binary sequence and estimate the most likely input value. These values are referred to as the log-likelihood ratios also called the soft decisions-having polarity and amplitude. The polarity of log likelihood ratios (LLR) value will provide the sign of the bit and amplitude will give the probability. The LLR value is calculated using:

\[ L(u_k|y) = \log \frac{\Pr(u_k = +1|y)}{\Pr(u_k = -1|y)} \]  

Where the numerator indicates the APP (A Posteriori Probability) of input sequence Ek. The turbo decoder performs the decoding action iteratively i.e., the MAP decoder1 performs decoding and then its values are passed to MAP decoder2 via interleaver, then the MAP decoder2 performs estimations after decoding and sends the same to MAP decoder1, thus first iteration is completed. These values obtained from serves as priori values for second iteration. Until the bit error rate is reduced to null or approximately null, the iterations are performed. The LLR values for forward, backward and branch metrics are calculated using the formula.

\[ \text{LLR}(u_k) = \log \left( \frac{\sum_{u_{k-1} = +1} \tilde{a}_{k-1}(s') \tilde{\beta}_{k}(s') \tilde{\gamma}_{k}(s', s)}{\sum_{u_{k-1} = -1} \tilde{a}_{k-1}(s') \tilde{\beta}_{k}(s') \tilde{\gamma}_{k}(s', s)} \right) \]  

\[ \tilde{a}_k(s) = \sum \tilde{\gamma}_k(s', s') \tilde{\beta}_{k-1}(s') \]  

\[ \tilde{\beta}_{k-1}(s') = \sum \tilde{\gamma}_k(s', s') \tilde{\beta}_k(s) \]  

IV. VITERBIDECODING ALGORITHM

The Viterbi algorithm applies the maximum likelihood principle to limit the comparison of so many surviving paths, to make the maximum likelihood decoding possible. It performs the maximum likelihood decoding but reduces the computational complexity by taking the advantage of the special structure of the code trellis. It is as shown in fig 3.
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The components in it include the adders, comparators and selector unit, hence the name ACS. The LUT (Look Up Table) is used to implement the logarithmic term as shown in Fig.6. In order to increase the processing speed, we are combining two radix2 units to form a radix4 [7] unit illustrated in Fig.7.

A. ACS Units

The forward and backward recursion computation is calculated using ACS architecture[3] as shown in Fig.4. The radix2 ACS architecture is shown in fig.5.

![Fig. 4. Basic Structure of ACS unit.](image)

![Fig. 5. ACS Unit for Radix-2.](image)

![Fig. 6. ACS Unit for Radix-4.](image)

![Fig. 7. Radix-4 ACS Unit with MSR Architecture.](image)

Then the, β and γ computations are as shown below Fig.8. According to trellis diagram, the node values are calculated as follows:

![Fig. 8. Basic trellis structure.](image)

B. Branch Metric Unit

A branch metric unit's function is as shown in fig: 9, to calculate branch metrics, which are normed distances between every possible symbol in the code alphabet, and the
received symbol. The branch metrics are difference values between received code symbol and the corresponding branch words from the encoder trellis.

![Diagram: BMC Unit](image)

**Fig. 9. BMC Unit.**

C. Survivor Path Unit

The survivor path unit stores the decisions of the ACS unit and uses them to compute the decoded output. The trace-back technique and the register-exchange approaches are two major techniques used for the path history management. The Trace back unit takes up less area but require much more time than the Register Exchange method. A relatively new approach called permutation network based path history unit implements directly the trellis diagram of the given Convolutional code to trace the survivor path back sequentially. The resulting circuit has smaller routing area than register-exchange technique and has faster decoding speed than trace-back method regardless of the constraint length.

**V. SIMULATION OF TURBO ALGORITHM**

The various modules of Convolutional encoder and Viterbi decoder in Verilog HDL is implemented here. The whole process of convolutional encoder and Adaptive Viterbi decoder can be summarized as shown in the flowchart of fig: 10.

![Flowchart: Adaptive Viterbi Decoder](image)

**Fig. 10. Flow Chart of Adaptive Viterbi Decoder.**

A. Example For The Viterbi Decoding Algorithm

In this below example the errors are present at the 2, 5, 7, 8th positions of the received signal. Then the errors present in the received signal can detect and corrected by the Viterbi Algorithm. From the fig: 11, the decoded signal from the Viterbi decoding Algorithm is given by 00 10 01 11.

![Diagram: Example of decoder path identification](image)

**Fig. 11. Example of decoder path identification.**

VI. RESULTS

Results of this paper is as shown in bellow Figs.12 to 16.

A. Results For Encoder

![RTL Schematic: Turbo encoder](image)

**Fig. 12. RTL Schematic of Turbo encoder.**

![Technical Schematic: Turbo Encoder](image)

**Fig. 13. Technical Schematic of Turbo Encoder.**

International Journal of VLSI System Design and Communication Systems
Volume.05, IssueNo.04, April-2017, Pages: 0350-0354
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VIII. REFERENCES


VII. CONCLUSION

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