Design and Implementation of Pulsed Latch Based Shift Register Using Body Biasing Techniques

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Abstract: This paper proposes a low-power shift register using pulsed latches with variable body biasing techniques. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. Instead of flip-flops we need to design the pulse latch circuit to design the shift registers with clock pulse generator. The variable body biasing reducing the static power consumption. The Simulation is done by Tanner EDA tool at 0.18um technology to reduce power dissipation.

Keywords: D-Latch, Pulse Generator, VBB.

I. INTRODUCTION

Most of the Flip-flops (FFs) are the memory storage elements extensively used in many digital designs. In particular, digital designs consisting of an intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and counters. It is also calculated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, which consumes 50% of the total system power. FFs thus contribute a major portion of the chip area and power consumption to the overall system design. The power dissipation is an important factor for the low power applications. The power optimization techniques are used at different levels of a digital design. The optimization at the logic level is one of the most necessary tasks for minimizing the power consumption. The latches and flip-flops are viewed as the critical logic components for the effectiveness of the digital circuits. They are widely used in the memory design, test applications and pipelines implementations. Since the power consumption depends on several parameters, different methods have been applied to reduce each of them. The processing speed of the system is doubled, if both clock edges have been used or the processing speed is preserved, if the circuit frequency becomes half. As the frequency becomes half it implies that the dynamic power of flip-flop and clock distribution network are half.

The circuit uses flip-flop with both clock edges. Due to increasing demand of battery operated portable handheld electronic devices like laptops, palmtops and wireless communication systems (personal digital assistants and personal communicators) the focus of the VLSI industry has been shifted towards low power and high performance circuits. Flip-flops and latches are the basic sequential elements used for realizing digital systems like shift Register. The flip-flops used in digital systems can be either dynamic or static based on their functionality when the clock is stopped/grounded, but the power is maintained. In this section I describe the related works of the projects. section II describe the proposed method section III analysis the results, & finally section IV describe the conclusion of the projects.

II. RELATED WORKS

A master-slave D flip-flop is created by connecting two gated D latches in series, and inverting the enable input to one of them. It is called master-slave because the second latch in the series only changes in response to a change in the first (master) latch.

Fig1. Master Slave Flipflop.

For a positive-edge triggered master-slave D flip-flop, when the clock signal is low (logical 0) the "enable" seen by the first or "master" D latch (the inverted clock signal) is high (logical 1). This allows the "master" latch to store the input value when the clock signal transitions from low to high. As the clock signal goes high (0 to 1) the inverted "enable" of the first latch goes low (1 to 0) and the value seen at the input to the master latch is "locked". Nearly simultaneously, the twice inverted "enable" of the second or "slave" D latch transitions from low to high (0 to 1) with the clock signal. This allows the signal captured at the rising edge of the clock by the now "locked" master latch to
pass through the "slave" latch. When the clock signal returns to low (1 to 0), the output of the "slave" latch is "locked", and the value seen at the last rising edge of the clock is held while the "master" latch begins to accept new values in preparation for the next rising clock edge.

**A. Pulse Latch Circuit**

The original SSASPL with 9 transistors is modified to the SSASPL with 7 transistors in Fig.2, by removing an inverter to generate the complementary data input (Db) from the data input (D). In the proposed shift register, the differential data inputs (D and Db) of the latch come from the differential data outputs (Q and Qb) of the previous latch. The SSASPL uses the smallest number of transistors (7 transistors) and it consumes the lowest clock power because it has a single transistor driven by the pulsed clock signal. The SSASPL was implemented and simulated with a 0.18µm CMOS process at VDD=1.8V. The sizes (W/L) of the three NMOS transistors (M1-M3) are 1µm/0.18µm. The sizes of the NMOS and PMOS transistors in the two inverters are all 0.5µm/0.18µm.

**B. Proposed Clock pulse Generator**

![Fig3. Clock Pulse Circuit.](image)

Each pulsed clock signal arrives at the sub shift registers at different time due to the pulse skew in the wire. The pulse skew increases proportional to the wire distance from the delayed pulsed clock generator. All pulsed clock signals have almost the same pulse skews when they arrive at the same sub shift register. Therefore, in the same sub shift register, the pulse skew differences between the pulsed clock signals are very small. The clock pulse intervals larger than the pulse skew differences cancel out the effects of the pulse skew differences. Another solution is to insert clock buffers and clock trees to send the short clock pulse with a small wire delay. But this increases the area and power overhead. Moreover, the multiple clock pulses make the more overhead for multiple clock buffers and clock trees.

**C. Proposed Shift Register**

![Fig5. Proposed shift register.](image)

A shift register is a clocked sequential circuit in which the binary word bits shift either towards left or towards right (towards higher place value or lower place value) on each successive clock transition. The pulse skew increases proportional to the wire distance from the delayed pulsed clock generator. All pulsed clock signals have almost the same pulse skews when they arrive at the same sub shift register. Therefore, in the same sub shift register, the pulse skew differences between the pulsed clock signals are very small. The clock pulse intervals larger than the pulse skew differences cancel out the effects of the pulse skew differences. Also, the pulse skew
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II. VARIABLE BODY BIASING

The proposed structures are combination of forced stack and sleep with variable body bias technique. The sleep transistor technique retains the logic state of circuit while forced stack maintains the minimum delay penalty. Thus this reduces the leakage power while saving the logic state. There are two modes of operation, active mode and sleep mode. The SSVBB has a structure merging forced sleepy stack with variable body biasing technique. The sleepy stack divides the existing transistors into two halves while maintaining the input capacitances. Then the sleep transistors are added in parallel to stacked pull up and pull down transistors. During active mode, $s=0$ and $s'=1$ are asserted, thus all sleep transistors are turned on thus reducing circuit delay. The performance is improved as the body to source of the PMOS is ON, which lowers the $V_{th}$ of PMOS transistor again. Due to body effect, $V_{th}$ decreases thus increases the performance. As the sleep transistors are always on there is faster switching time than the forced stack. During sleep mode, $s=1$ and $s'=0$ are asserted, so both of the sleep transistor are turned off, thus maintaining the logic state of the circuit. As a result of body effect, $V_{th}$ increases, which decrease the performance.

IV. RESULTS

Table 1.

<table>
<thead>
<tr>
<th>Types</th>
<th>Power consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without Body biasing</td>
<td>1.475e-003 watts</td>
</tr>
<tr>
<td>With body biasing</td>
<td>5.785691e-004 watts</td>
</tr>
</tbody>
</table>

V. CONCLUSION

The shift register reduces area and power consumption by replacing flip-flops with pulsed latches using Variable body biasing. A 20-bit shift register was implemented using a 0.18 um CMOS technology with $vdd=1.8V$ at clock frequency of 100 MHz, which consumed the power and area compared to conventional method that is shift register using flip flops.

VI. REFERENCES


