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FPGA Implementation of Multiband Clock Distributation using VLSI Technology

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Abstract: The clock distribution network consumes nearly 70% of the total power consumed by the integrated circuit since this is the only signal which has the highest switching activity. Normally for a multiband clock domain network we develop a multiple PLL, this project aim for developing a low power single clock multiband network which will supply for the multi clock domain network. This project is highly useful and recommended for communication applications like Bluetooth, Zigbee. WLAN frequency synthesizers are proposed based on pulse-swallow topology and the designed is modeled using Verilog simulated using Modelsim and implemented and synthesized using Xilinx tool.

Keywords: FPGA, WLAN, Bluetooth, Zigbee, Verilog.

I. INTRODUCTION

Wireless LAN (WLAN) in the multi gigahertz bands, such as HIPER LAN II and Network standards like a 802.11a/b/g, are recognized as leading standards for high-rate data transmissions, and standards like Network protocol 802.15.4 are recognized for low-rate data transmissions. The integrated synthesizers for Wireless LAN applications at 5 GHz reported in and consume up to 24 mw in CMOS realizations, where the first-stage divider is implemented using an Injection-locked divider which consumes large chip area and has a narrow locking range. The best published frequency synthesizer at 5 GHz consumes 9.6 mw at 1-V supply, where its complete divider consumes power around 6 mw, where the first-stage divider is implemented using the source-coupled logic (SCL) circuit, which allows higher operating Frequencies but uses more power. Dynamic latches are faster and consume less power compared to static dividers. High speed divide-by- counter (also called prescaler) is a fundamental module for frequency synthesizers. Its design is crucial because it operates at a higher frequency and consumes higher power consumption. A divide-by- counter consists of flip-flops (FF) and extra logic, which determines the terminal count. Conventional high speed FF based divide by counter designs use current-mode logic (CML) latches and suffer from the disadvantage of large load capacitance.

This not only limits the maximum operating frequency and current-drive capabilities, but also increases the total power consumption. Alternatively, FF based divide-by designs adopt dynamic logic FFs such as true-single-phase clock (TSPC). The designs can be further enhanced by using extended true-single-phase-clock (E-TSPC) FFs for high speed and low power applications . E-TSPC designs remove the transistor stacked structure so that all the transistors are free of the body effect. They are thus more sustainable for high operating frequency operations in the face of low voltage supply. Past optimization efforts on prescaler designs focused on simplifying the logic part to reduce the circuit complexity and the critical path delay. For example, an E-TSPC design embedded with one extra P-MOS/N-MOS transistor can form an integrated function of FF and AND/OR logic . Moving part of the control logic to the first FF to reduce unnecessary FF toggling yields another version of prescaler design .These two classic designs each contains 16 transistors only and the mode control logic uses as few as 4 transistors. To achieve such circuit simplicity, it calls for a rationed structure in the FF design. Despite its distinct speed performance, the incurred static and short circuit power consumptions are significant. Latest designs presented in adopt a general TSPC logic family containing both rationed and ratio less inverter alternatives. Since the maximum height of transistor stacking is up to 5, these designs lose their performance advantages when working under a low scenario.

In a power gating technique by inserting an extra PMOS between and the FF is employed in two novel divide-by-2/3 counter designs. The unused FF can be shut down when working in the divide-by-2 mode. Due to the increase in the number of transistor stacking (up to 4), these designs are not suitable for low operations. Due to the quadratic dependence of power consumption on supply voltage, lowering is a very effective measure to reduce the power at the expense of speed performance. .In particular, here focus on low operations for power saving without sacrificing the speed performance. In this design, rationed E-TSPC FFs are employed due to its circuit simplicity and speed performance. Only one pass transistor is needed to implement the mode control logic. The proposed design in capable of working at a maximum frequency of 531 MHz when the supply voltage is as low as 0.6 V.

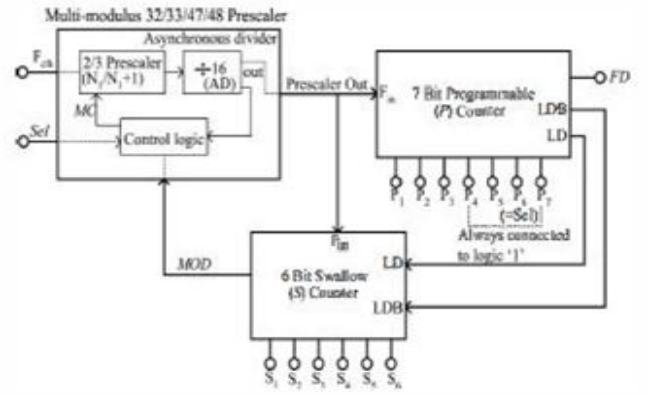


Fig1. Proposed dynamic logic multiband flexible divider.

The TSPC and E-TSPC designs are able to drive the dynamic latch with a single clock phase and avoid the skew problem. However, the adoption of single-phase clock latches in frequency dividers has been limited to PLLs with applications below5 GHZ. The frequency synthesizer reported in [6] uses an E-TSPC prescaler as the first-stage divider, but the divider consumes around 6.25 mw. Most Network protocol 802.11a/b/g frequency synthesizers employ SCL dividers as their first stage, while dynamic latches are not yet adopted for multiband synthesizers. In this paper, a dynamic logic multiband flexible integer-N divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler and a wideband multi modulus 32/33/47/48 prescaler as shown in Fig. 1. The divider also uses an improved low power loadable bit-cell for the Swallow-counter.

II. DESIGN CONSIDERATIONS

The key parameters of high-speed digital circuits are the propagation delay and power consumption. The maximum operating frequency of a digital circuit is calculated and is given by

$$f\ max = 1/tpLH+tpH\ L \quad (1)$$

Where tpLH and tpHL are the propagation delays of gates, respectively. The total power consumption of the CMOS digital circuits is determined by the switching and short circuit power. The switching power is linearly proportional to the operating frequency and is given by the sum of switching power at each output node as in

$$P_{\text{switching}} = \sum_{i=1}^{n} f_{\text{clk}} C_{Li} V_{\text{dd}}^2 \quad (2)$$

Where n is the number of switching nodes fclk is the clock frequency cli is the load capacitance at the output node of the stage, and Vdd is the supply voltage. Normally, the short-circuit power occurs in dynamic circuits when there exists direct paths from the supply to ground which is given by

$$P_{\text{sc}} = I_{\text{sc}} * V_{\text{dd}} \quad (3)$$

where Isc is the short-circuit current. The analysis in shows that the short-circuit power is much higher in E-TSPC logic circuits than in TSPC logic circuits. However, TSPC logic circuits exhibit higher switching power compared to that of E-TSPC logic circuits due to high load capacitance. For the E-TSPC logic circuit, the short-circuit power is the major problem. The E-TSPC cicuit has the merit of higher operating frequency than that of the TSPC circuit due to the reduction in load capacitance, but it consumes significantly more power than the TSPC circuit does for a given transistor size. The following analysis is based on the latest design using the popular and low-cost 0.18-_m CMOS process.

III. WIDEBAND E-TSPC 2/3 PRESCALER

The E-TSPC 2/3 prescaler consumes large short circuit power and has a higher frequency of operation than that of TSPC 2/3 prescaler. The wideband single-phase clock 2/3 prescaler used in this design do not consist of two D-flip-flops and two NOR gates embedded in the flip flops. The first NOR gate is embedded in the last on DFF1, and the second NOR gate is embedded in the first stage of DFF2.

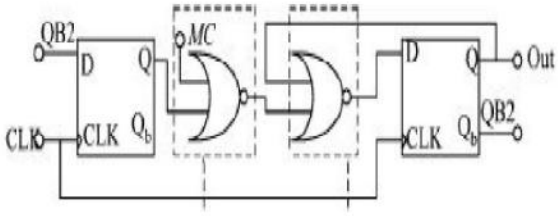


Fig2. Wideband single-phase clock 2/3 prescaler.

The first NOR gate is embedded in the last stage of DFFI, and the second NOR gate is embedded in the first stage of DFF2 The switching of division ratios between 2 and 3 is controlled by logic signal MC. The load capacitance of the prescaler is given by

$$C_{L\text{-wideband}}=C_{dbM19}+2C_{gdM19}+C_{dbM21}+2C_{gdM21}+C_{Gm1} \quad (4)$$

When MC switches from "0" to "I," transistors M2,M4 and Ms in DFF 1 turns off and nodes S I, S2 and S3 switch to logic "0." Since node S3 is "0" and the other input to the NOR gate embedded in DFF2 is Qb, the wideband prescaler operates at the divide-by-2 mode. During this mode, nodes S I, S2 and S3 switch to logic "0" and remain at "0" for the entire divide-by-2 operation, thus removing the switching power contribution of DFFI. Since one of the transistors is always OFF in each stage of DFFI, the short-circuit power in DFFI and the first stage of DFF2 is negligible. The total power consumption of the prescaler in the divide-by-2 mode is equal to the switching power in DFF2 and the short-circuit power in second and third stages of DFF2 and is given by

$$C_{L\text{-wideband}}=C_{dbM19}+2C_{gdM19}+C_{dbM21}+2C_{gdM21}+C_{Gm1} \quad (5)$$

When MC switches from "0" to "I," transistors M2,M4 and Ms in DFF 1 turns off and nodes S I, S2 and S3 switch

to logic "0." Since node S3 is "0" and the other input to the NOR gate embedded in DFF2 is Qb, the wideband prescaler operates at the divide-by-2 mode. During this mode, nodes S I, S2 and S3 switch to logic "0" and remain at "0" for the entire divide-by-2 operation, thus removing the switching power contribution of DFFI. Since one of the transistors is always OFF in each stage of DFFI, the short-circuit power in DFFI and the first stage of DFF2 is negligible. The total power consumption of the prescaler in the divide-by-2 mode is equal to the switching power in DFF2 and the short-circuit power in second and third stages of DFF2 and is given by

$$P_{widebanb\text{-}divide\text{-}by\text{-}2}=\sum f_{clk}C_{Li}V_{dd}^{2}+P_{SC1}+P_{SC2} \quad (6)$$

Where Cli is the load capacitance at the output node of the ith stage of DFF2, and PSCI and PSC2 are the shortcircuit power in the second and third stages of DFF2. When logic signal MC switches from "I "to "0," the logic value at the input of DFFI is transferred to the input of DFF2 as one of the input of the NOR gate embedded in DFFI is "0" and the wideband prescaler operates at the divide-by-3 mode. During the divide-by- 2 operation, only DFF2 actively participates in the operation and contributes to the total power consumption since all the switching activities are blocked in DFFI. Thus, the wideband 2/3 prescaler has benefit of saving more than 50% of power during the divide-by-2 operation. The measured results shows that the wideband 2/3 prescaler has the maximum operating frequency of 6.5GHz.

IV. MULTIMODULUS 32/33/47/48 PRESCALER

The proposed wideband multimodulus prescaler which can divide the input frequency by 32, 33, 47, and 48 is shown in Fig. 4. It is similar to the 32/33 prescaler used in , but with an additional inverter and a multiplexer. The proposed prescaler performs additional divisions (divide-by-47 and divide-by-48) without any extra flip flop, thus saving a considerable amount of power and also reducing the complexity of multi band divider.

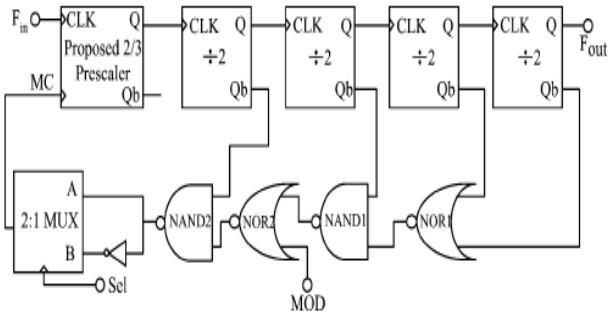


Fig3. Proposed Multimodulus 32/33/47/48 Pres caler.

The multimodulus prescaler consists of the wideband 2/3 (N/(N]+I)) prescaler, four asynchronous TSPC divide-by-2 circuits ((AD)=16) and combinational logic circuits to achieve multiple division ratios. Beside the usual MOD signal for controlling N/(N+l) divisions, the additional control signal sel is used to switch the prescaler between 32/33and 47/48 modes.

Case 1: sel='O'

When sel='O', the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal MOD. If MC=I, the 2/3 prescaler operates in the divide-by-2 mode and when MC=O, the 2/3 prescaler operates in the divide-by-3 mode. If MOD=I, the NAND2 gate output switches :to logic "I" (MC=I) and the wideband pres caler operates in the divide-by-2 mode for entire operation. The division ratio N performed by the multi modulus prescaler is

$$N = (AD*N1])+(O*(N1+ 1)) = 32 \quad (7)$$

Where N1=2 and AD=16 is fixed for the entire design. If MOD=O , for 30 input clock cycles MC remains at logic "1", where wideband prescaler operates in divide-by-2 mode and, for three input clock cycles, MC remains at logic "0" where the wideband prescaler operates in the Divide-by-3 mode. The division ratio N+ 1 performed by the multi modulus prescaler is and

$$N+l = ((AD-l)*N) +(1*(N1+1)) = 33 \quad (8)$$

S2 switch to logic "0" and the bit-cell does not perform any function. The MOD signal goes logically high only when the S-counter finishes counting down to zero. If MOD and LD are logically low, the bit-cell acts as a divide-by-2 unit. If MOD is logically low and LD is logically high, the input bit PI is transferred to the output. In the initial state, MOD=O, the multimodulus prescaler selects the divide-by-N+ 1 mode (divide-by-33 or 2)

Case 2: sel =' l'

When sel = ' 1', the inverted output of the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescalar operate as a 47/48 prescaler, where the division ratio is controlled by the logic signal MOD. If MC= 1, the 2/3 prescaler operates individe-by- 3 mode and when MC=O, the 2/3 prescaler operates individe-by-2 mode which is quite opposite to the operation performed when sel='O' If MOD=I, the division ratio N+ 1 performed by the multimodulus prescaler is same except that the wideband prescaler operates in the divide by-3 mode for the entire operation given by

$$\mathbf{N+l =(AD*(N1+1))+(0*Nl) =48}$$

If MOD=I, the division ratio N performed by the multimodulus prescaler is

$$\mathbf{N = ((AD-l)*(N1+1))+(1 * Nl) = 47}$$

V. MULTTBAND FLEXIBLE DIVIDER

The single-phase clock multiband flexible divider which is shown in Figl.l consists of the multi modulus 32/33/47/48 prescaler, a 7-bit programmable P-counter and a 6 bit swallow S-counter. The control signal Sel decides whether the divider is operating in lower frequency band (2.4 GHz) or higher band (5-5.825 GHz).

A. .Swallow (S) Counter

The 6-bit s-counter shown in Fig.4. consists of six asynchronous loadable bit-cells, a NOR-embedded DFF and additional logic gates to allow it to be programmable from 0 to 31 for low-frequency band and from 0 to 47 for the high-frequency band. The
asynchronous bit cell used in this design .It is similar to the bit-cell except it uses two additional transistors M6 and M7whose inputs are controlled by the logic signal MOD. If MOD is logically high, nodes S 1

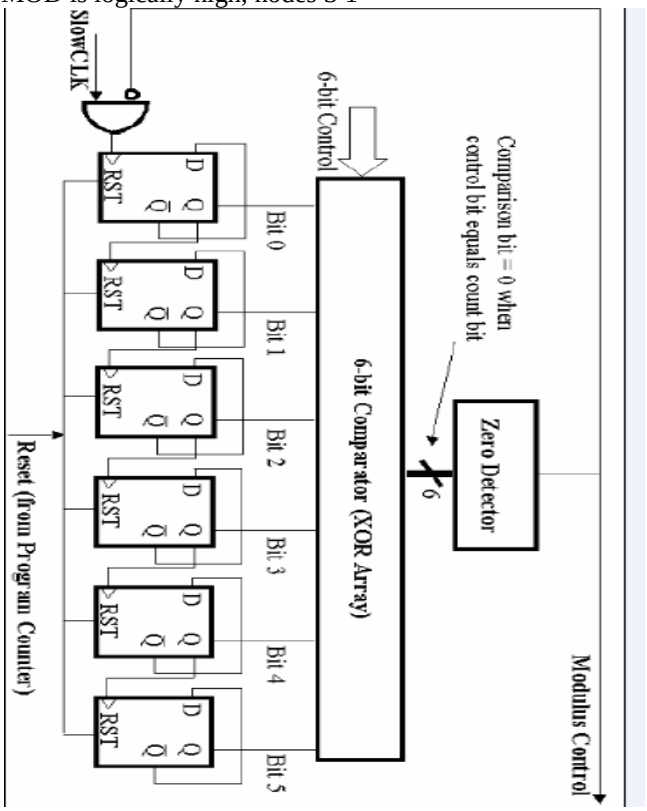


Fig4. Swallow(S) Counter.

divide-by-48) and P, S counters start down counting the input clock cycles. When the S-counter finishes counting, MOD switches to logic "1" and the prescaler changes to the divide-by-n mode (divide-by-32 or divide-47) for the remaining P-S clock cycles. During to a specified value from 0 to 31 for the lower band and o to 48 for the higher band of operation. this mode, since S-counter is idle, transistors M6 and M7 which are controlled by MOD, keep the nodes S 1 and S2 at logic "0," thus saving the switching power in S counter for a period of (N*(P-S)) clock cycles. Here, the programmable input (PI) is used to load the counter.

B. Programmable (P) Counter

The programmable P-counter is a 7-bit asynchronous down counter which consists of 7 loadable bit-cells and additional logic gates. Here, bit P7 is tied to the Sel signal of the multi modulus prescaler and bits P 4 and P7 are always at logic "1." The remaining bits can be externally programmed from 75 to 78 for the lower frequency band and from 105 to 122 for the upper frequency band. When the P-counter finishes counting down to zero, LD switches to logic "1" during which the output of all the bit-cells in S-counter switches to logic "1" and output of the NOR embedded DFF switches to logic "0" (MOD=O) where the programmable divider get reset to its initial state and thus a fixed division ratio is achieved. If a fixed 32/33 (N/(N+ 1)) dual-modulus prescaler is used, a 7bit P counter is needed for the low-frequency band (2.4 GHz) while an 8-bit S-counter would be needed for the high frequency band(5-5.825 GHz) with a fixed 5-bit S counter. Thus, the multimodulus32/33/47/48 prescaler eases the design complexity of the P-counter.

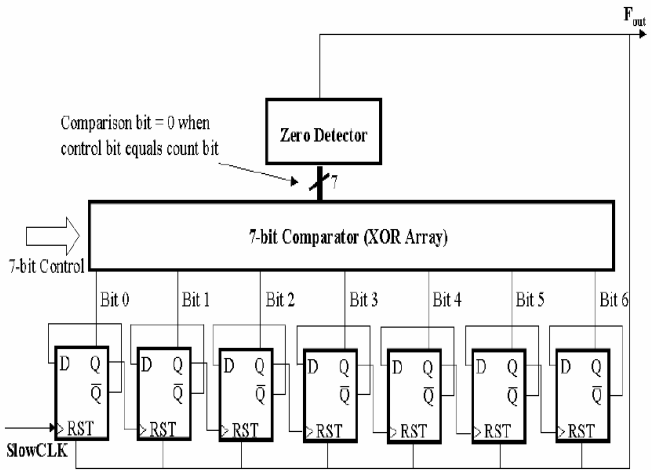


Fig5. Programmable (P) Counter.

V .RESULTS AND CONCLUSION

Tab Le-I: Prescaler Frequency Divide Ratios

Sel	MOD	MC	MODE
0	1	1	Divide-by-2
	0	1	Divide-by-2
	0	0	Divide-by-3
1	1	0	Divide-by-2
		1	Divide-by-3

1. When Sel='O':

When Sel='O' the output from N4 gate is given to the prescaler and the multimodal's prescaler selects 32/33 mode and the division ratio is controlled by MOD signal. When MOD=1 the output from N4 gate switches to logic' 1 ' and the prescaler operates in divide-by-2 for entire operation. i.e., now division ratio of 32 (N) is performed. Similarly when MOD=O, MC remains high for first 30 input clock cycles and goes low for 3 input clock cycles. Thus division ratio of 33(N+ 1) is performed. N and N+ 1 are given by

$$N = (AD * N1) = 32$$

$$N + 1 = ((AD - 1) * N1) + (1 * (N1 + 1)) = 33$$

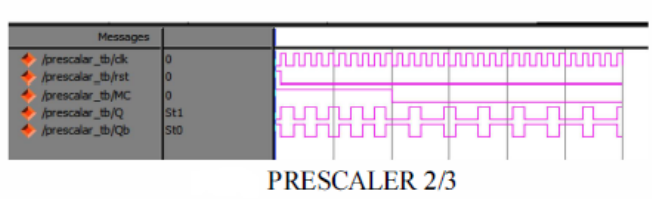
2. When Sel=l:

When Sel=l, the inverted output from N4 gate is given to the input of 2/3 prescaler and multimodal's prescaler operates in 47/48 mode. MOD signal controls the division ratio. When MOD=1 and MC=1 prescaler operated in divide-by-3 for the entire input cycles and division ratio of 48 (N+l) is performed. When MOD=1 and MC=O divideby-2 is selected for entire input clock cycles for prescaler and the division ratio of 47(N) is performed. N and N+l are given by

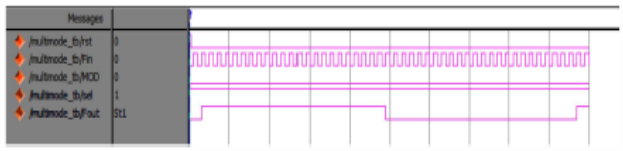
$$N = ((AD - 1) * (N1 + 1)) + (1 * 2\ N1) = 47$$

$$N + 1 = (AD * (N1 + 1)) = 48$$

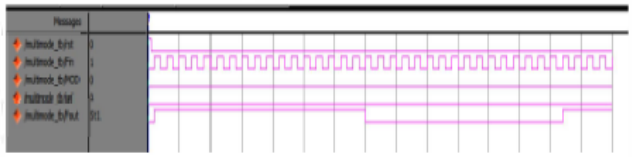
VI. SIMULATED RESULT



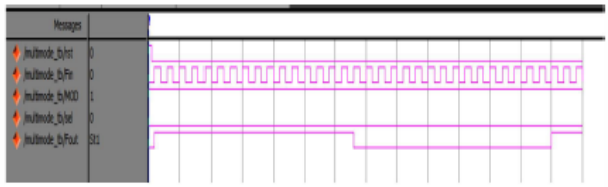
PRESCALER 2/3



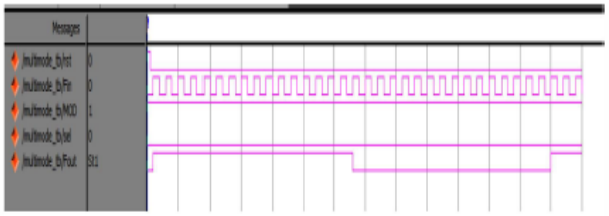
DIVIDE-BY-32



DIVIDE-BY-33



DIVIDE-BY-47



DIVIDE-BY-48

6..CONCLUSION

In this paper a simple approach for the low power single phase clock distribution for Wireless Local Area Networks frequency synthesizer is presented. The technique for low power fully programmable divider using design of bit cells for P and S Counter is given. P and S counters can be programmed accordingly for the required bands of frequencies. Here the clock divider uses a wide band 2/3 prescaler and a multimodal's prescaler. By using this multimodal's prescaler.

VII. REFERENCE

[1] H.R.Rategh et al., "A CMOS frequency synthesizer with an injected locked frequency divider for 5-GHz wireless LAN receiver," IEEE J. Solid-State Circuits, vol. 35, no. 5, pp. 780-787, May 2000.

[2] P. Y. Deng et al., "A 5 GHz frequency synthesizer with an injection locked frequency divider and differential switched capacitors," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 56, no. 2, pp. 320-326, Feb. 2009.

[3] L. Lai Kan Leung et al., "A I-V 9.7-mW CMOS frequency synthesizer for IEEE 802.lIa transceivers," IEEE Trans. Micro wind. Theory Tech., vol. 56, no. I, pp. 39-48, Jan. 2008.

[4] M. Alioto and G. Palumbo, Model and Design of Bipolar and MOS Current-Mode Logic Digital Circuits. New York: Springer, 2005.

[5] Y. Jorgen etc all, "A true single-phase-clock dynamicCMOScircuit technique," IEEE J. Solid-State Circuits, vol. 24, no. 2, pp. 62-70, Feb. 1989.

[6] S. Pellerano etc, "A J3.5-mW 5 GHz frequency synthesizer with dynamic-logic frequency divider, " IEEE J. Solid-State Circuits, vol. 39, no. 2, pp. 378-383, Feb. 2004

[7] V. K. Manthena etc aIl, "A low power fully programmable J MHz resolution 2.4 GHz CMOS PLL frequency synthesizer, " in Proc. IEEE Biomed. Circuits Syst. Conf, Nov. 2007.pp 187-19 .