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Implementation of Intelligence Traffic Light Controller Based on FPGA with VHDL

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Abstract: Traffic lights are the signaling devices used to manage traffic on multi-way road. These are positioned to control the competing flow of the traffic at the road intersections to avoid collisions. By displaying lights (red, yellow and green), they alternate the way of multi-road users. The implementation of traffic Light Controller can be through a Microcontroller, Field Programmable Gate Array or Application Specific Integrated Circuit. FPGA implementation is advantageous over ASIC and microcontroller; number of IO ports and performance compared to microcontroller and implementation with FPGA is less expensive compared to ASIC design. This paper presents the FPGA implemented low cost advanced TLC system using Chip Scope Pro and Virtual Input Output. The TLC implemented is one of the real and complex signaling lights in Kingdom of Bahrain, for pedestrian way included four roads and sensors and camera assisted motorway. The system has been implemented in hardware using Spartan-3E FPGA.

Keywords: FPGA, Xilinx, VHDL, VLSI, TLC (Traffic Light Controller).

I. INTRODUCTION

Through using VHDL language to the traffic light controller design, the traffic light control circuit uses digital signal automatic control to realize two groups of lights which are red, yellow and green. Those lights command vehicles and pedestrians passing safely at the crossroad, which bases on the data of traffic state transition. Most of control systems are made by advanced PLC (Programmable Logic Controller) technology, which even can effectively imitating the experienced traffic policeman‘s thought. In addition, FPGA cannot compare the Anti-dry round benefit and fast speed benefit. However, PLC has a disadvantage for traffic light design. Most PLC costs more than $400(could be 10 times of FPGA cost), which has not considered the expansion module. The PLC technology is mostly used in heavy industry and Precision Instruments production. There are two kinds of the VHDL design, which are modeling and synthesis. The modeling VHDL design has significant advantage in complicated system design. In addition, the VHDL should not be thought as a programming language. This language is designed to describe the logic circuit. A classic model is a very helpful point to start programming the project. The FPGA traffic light control system needs to consider the current traffic situation, which is base on the data from sensors. The FPGA gets current signals of vehicles passing crossroad and base on those signals send next step order. Also, in the specific road the traffic light should be set specifically. In addition, the FPGA need to consider the time, which means separating the traffic situation by the time.

In the FPGA programming the codes should be packaged base on different models, which could increase he programs' flexibly. The states machine is good way to separate the system to different function model. Also, the states machine is easy to realize in VHDL language. An advanced system should include traffic lights controller, countdown controller and LED display controller. Led display showing the countdown time which give the driver a directly time conception to reduce the probability of traffic accident. According to the simulation phase, the time split module is necessary based on the real-life requirement. The traffic congestion due to the exploding increase of vehicles became the severest social problems and it has a major effect on the economy of a country. Therefore, many researches about traffic light system have been done in order to overcome some complicated traffic phenomenon but existent research had been limited about present traffic system in well-travelled traffic scenarios. The time of allocation is fixed from east to west or opposite way and from north to south way in crossroads. Field Programmable Gate Arrays (FPGAs) are extensively used in rapid prototyping and verification of a conceptual design and also used in electronic systems when the mask-production of a custom IC becomes prohibitively expensive due to the small quantity. Many system designs that used to be built in custom silicon VLSI are now implemented in Field Programmable Gate Arrays. This is because of the high cost of building a mask production of a custom VLSI especially for small quantity.

II. TRAFFIC LIGHT CONTROL SYSTEM DESIGN

In the traffic lights design, the external hardware includes two sets of traffic lights and two LED displays (Fig.1 draws the east - west and north-south traffic light and LED display). The software system bases on:

A. Circuit Synthesis Module Concept

The traffic signal system is divided into several small circuits. Each module is written in VHDL codes. Those small circuits also connect together. This subdivided working design increases the speed of debugging and programming (see Fig.1).

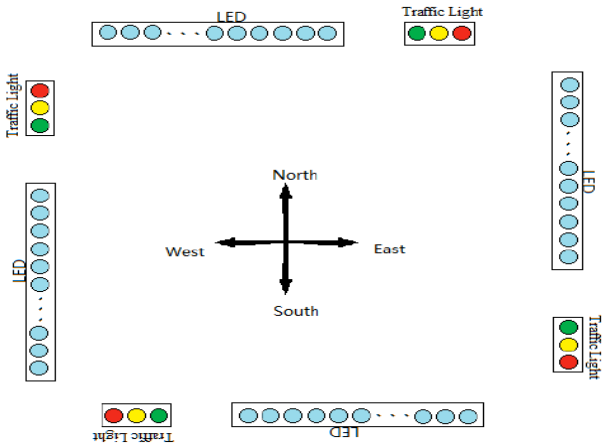

Fig.1. Schematic diagram of crossroads.

B. Parameterization Concept

The traffic light circuit can be adjusted by the time (increase or decrease the count time in circuit) to increase the flexibility of process.

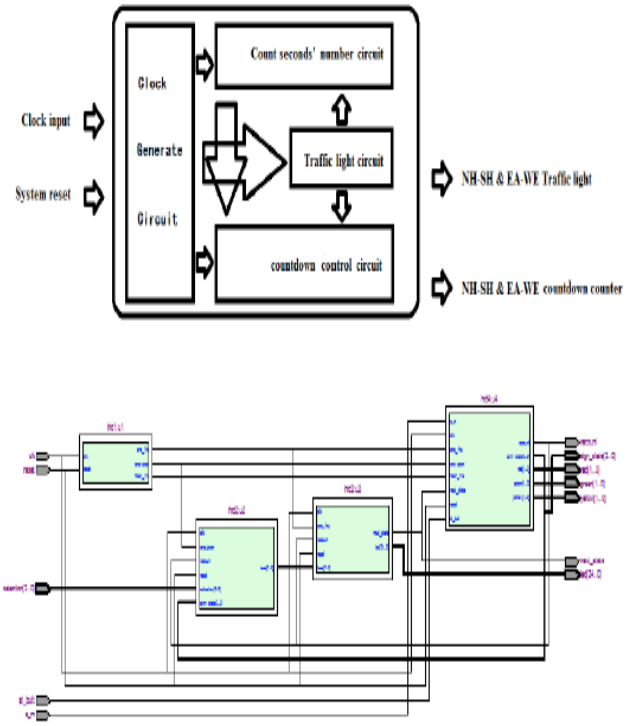

Fig.2. Traffic signal light system structure.

At the traffic lights signal system, it is most likely to use the automatic control mode. In order to avoid the occurrence of accidents the circuit must be given a stable clock to make system working normally. Therefore, the hld1 clock circuit (see Fig.2) main function is to produce a stable output signal which is used as several circuits' enabling control and synchronization signal.

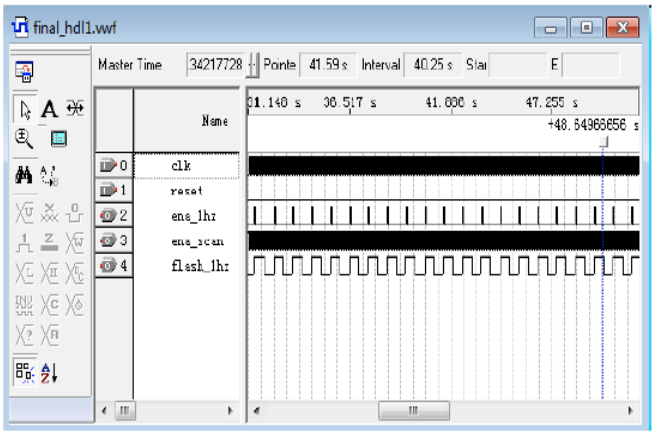

Fig.3. Clock generation circuit diagram.

In Fig.3, the external signal generator provides 1kHZ clock signal then the output signal scan system splits this clock signal's frequency. "ena_1hz" produces a cycle of pulse signal each second. "flash_1hz" produces a 1Hz pulse clock signal. The special point during the design process is using constant parameter. The intention of using constant parameter is in order to make the program easier to read and modify. Changing the values of the constants updates constant's value for whole program, which enhance the flexibility of this project. In addition, at the programming process all of the constant parameters inputs and outputs are given some evident names. It increases efficiency of debugging and makes the project easy to be fixed by another programmer, because the function of every part is obvious. On the crossroads, a countdown display for vehicles and pedestrians in one direction may raise passing efficiency. Therefore, main function of "hld2", which is the number of seconds count selection circuit (see Fig. 1), is producing the required digital display (i.e. the numerical seconds countdown). This number is used on the countdown display circuit's output.

Description of choice by counting the timing diagram circuit (see Fig.3): this program defines in normal traffic. Under this condition, the maintain time of red light vector, yellow light vector and the green light vector are 15s, 5s and 25s on both meridional and trans meridional direction. Base on the real life experience, some traffic light already use the countdown display. Their role is telling the vehicles and pedestrians how much time they have by the traffic signal changing. So, the vehicles and pedestrians know whether there is enough time to pass the intersection, which can avoid some accidents. For example, when north-south direction is green, vehicles run normally in this direction. And, the vehicle is waiting for red light vectors in east-west direction.

If the vehicles in north-south direction realize no passing by the countdown display, they could slow down and wait for the next pass. The vehicle in the east-west direction can run normally without wait for the north-south direction vehicle. The crossroads will run smoothly. Considering the traffic jam makes vehicles waiting in a long line and some drivers are difficult to see the countdown display clearly, which may affect vehicles running. Therefore, the light vector-emitting diode countdown is realizable for the drivers and pedestrians even a mile away. The main function of Signal_Light_vector3 countdown control circuit (see Fig.3) is receiving Signal_Light_vector2 circuit output value, and converting it to be BCD code which is used in light vector-emitting diode display. The vehicles and pedestrians can clearly know how long time left before the lights changing.

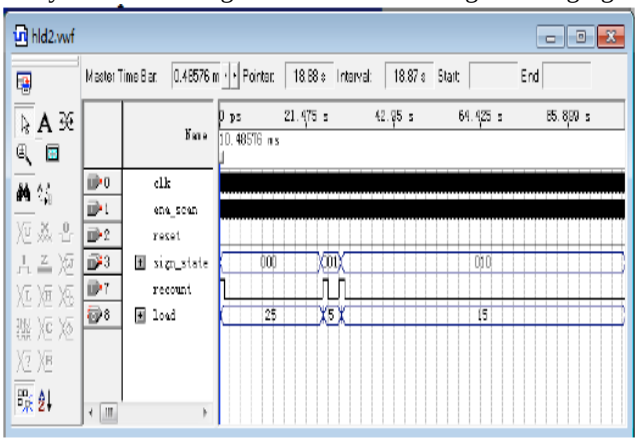

Fig.4. Second number counters selection.

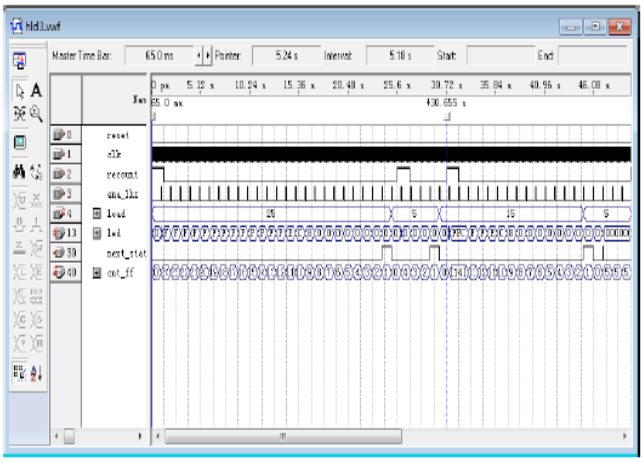

Fig.5. Countdown timing control circuit diagram.

This program is the using of look-up table method and light vector-emitting diodes (LED) to realize the countdown displaying. In when the internal counter start counting, the green lamp light, and load minus1 and put it into COUNT_ff. And then, COUNT_ff pointed the corresponding value in the case statement transmit which drives the LED displaying the remaining time. The conv_integer () also be used in the programming. It can convert COUNT_ff's value (assigned) to integer. From the Fig.5, LED is a 25 bit signal output, which controls the output light vector emitting diode.

This 25 bit output signal can be displayed by seven groups control LED which uses "1" to "0" to extinguish the light vector. The program code in Appendix 3 is countdown control circuit. Most traffic light systems use the automatic control mode to direct the traffic. But, in order to prevent traffic congestion during the rush hour sometimes the manual control is required, which give policemen ability to direct the traffic. Therefore, "hld4" traffic signal control circuit main function is to switch manual and automatic mode. Police officers could control the traffic light signal system operation by the external input as shown in Fig.6.

According to the chart: when a_m=1 (the automatic mode) the next state can be triggered.

- Red, Green, Yellow was 01, 10, 00, when rewgsn=1. At this state, working light vectors are red ones for east-west direction (red = 01) and the green ones for north-south direction (green = 10).
- Red, Green, Yellow was 01, 00, 10, when rewysn=1. At this state, working light vectors are red ones for east-west direction (red = 01) and the yellow ones for north-south direction (yellow = 10).
- Red, Green, Yellow was 10, 01, 00, when gewrsn=1. At this state, working light vectors are green ones for east-west direction (Green = 01) and the red ones for north-south direction (red = 10).
- When next_state_butt = 1, the state automatic switches to manual (auto_manual=0). Since reset = 1, Red, Green, Yellow is changed from 10, 01, 00 to 01, 10, 00 (i.e. red light vector for east-west direction, green light vector north-south direction, the initial state).

The hld5 circuit's job is to connect all of the sub circuits and process the timing analysis as shown in Figs.7 and 8. When the process is completed, downloaded it to the FPGA and finished the hardware circuit verification.

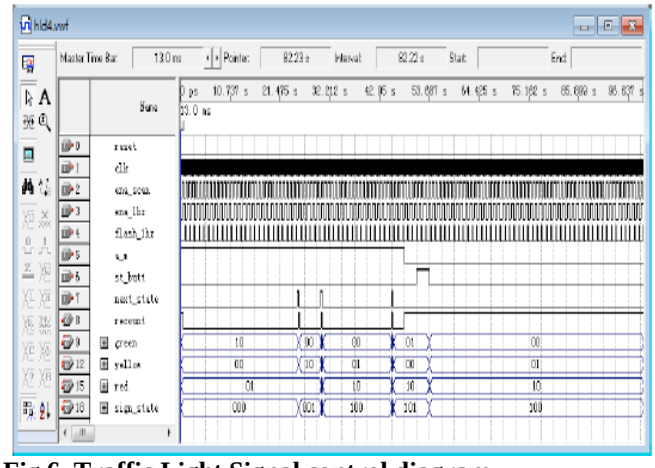

Fig.6. Traffic Light Signal control diagram.

In most programming languages, at the beginning the program always calls the library to provide the basic procedure command. However, if it is a complex program, library commands might not support completely. Therefore, a subroutine is required for programming. This problem also

exists in hardware description language (VHDL). In VHDL program's the first row (Library IEEE ;) is to use IEEE's library files in purpose. But, if the device is not in the library, that device has to be definite by user. A package should contain at least one of the following structures:

- **Constant Description:** the channel to define the width of system data bus.
- **The VHDL data type specification:** mainly used to organize the general data type in the whole design.
- **The element definition:** Provision the VHDL elements involved in design file at the port define interface.
- **The subroutine:** subprograms are incorporated into the package, which makes them easy to be called in different parts of the design.

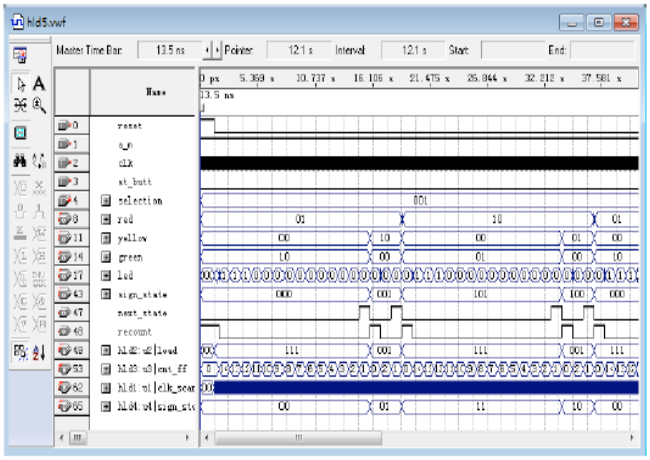

Fig.7.The timing diagram of after connected each module.

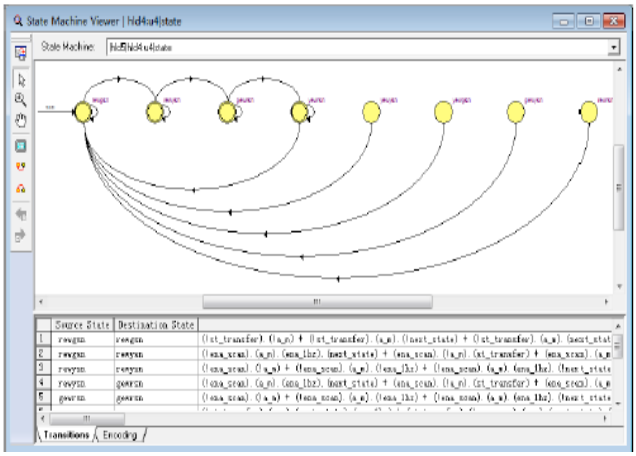

Fig.8. The timing diagram after connection.

III. STATE DIAGRAM

The TLC state diagram shown in Fig. 9 illustrates that whenever cnt=00 and dir=00,then green light in north direction will be ON for few seconds and red signal light in all other directions namely west, south and east will be ON. When cnt=01 and dir=00 then yellow light (y1) will be ON for few seconds and when cnt=01 yellow light (y2) and pedestrian north will be ON and then dir is incremented by one and cnt is assigned to zero. So when cnt=00 and dir=01, the green light in east direction will be ON for few seconds and all red lights in other directions be ON.

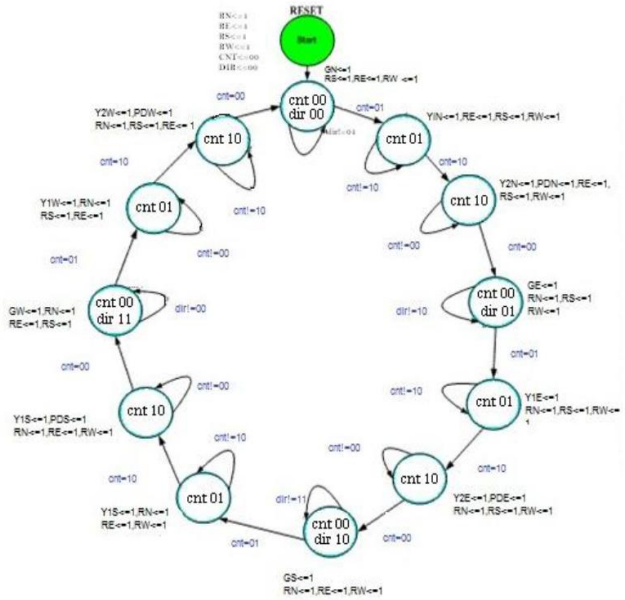

Fig.9. TLC State Diagram.

TABLEI. Terms used in State Diagram

South	West
GS= green south RS= right south Y1S=yellow light1south Y2S= yellow light 2 south PDS=pedestrain south	GW = green west RW = right west Y1W = yellow light 2 west Y2W = yellow light 2 west PDW = pedestrain west
North	**East**
GN = green north RN = red north Y1N = yelow light 1 east Y2N = yellow light 2 north PDN = pedestrain north	GE = green east RE = red east Y1E = yellow light 2 east Y2E = yellow light 2 east PDE = pedestrain east

Whenever cnt=01 and dir=01 then yellow light (y1) will be ON for few seconds and when cnt=01 yellow light (y2) and pedestrian east will be ON and then dir is incremented by one and cnt is assigned to zero. So whenever cnt=00 and dir=10, the green light in south direction will be ON for few seconds and all red lights in other directions will be ON. Whenever cnt=01 and dir=10 then yellow light (y1) will be ON for few seconds and when cnt=01 yellow light (y2) and pedestrian south will be ON and then dir is incremented by one and cnt is assigned to zero. So whenever cnt=00 and dir=11, the green light in west direction will be ON for few seconds and all red lights in other directions will be ON. Whenever cnt=01 and dir=11 then yellow light (y1) will be ON for few seconds and when cnt=01 yellow light (y2) and pedestrian west will be ON and then dir is assigned to 00 and cnt is assigned to zero. This sequence repeats and the traffic flow will be controlled by assigning time periods in all the four directions. Table I specifies the abbreviations used in TLC state diagram. Labeling for each lane is done by assigning the direction label in order to distinguish the outputs from each other with their states. In the traffic light controller program there will be two inputs namely clock and reset. When the two variables are „1" then the TLC will start working.

Initially that is when reset is „0" then the red signal lights in all the directions will be ON and when reset is „1", then the traffic light controller system will be on assigning cnt and dir variables to 00 where cnt and dir respectively represent the states and the four directions in the state machine.

IV. SIMULATION AND FPGA IMPLEMENTATION

Simulation and FPGA Implementation results of this paper is shown in bellow Figs.15.

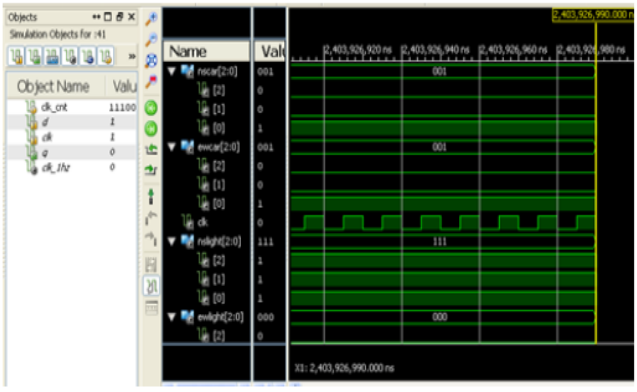

Fig.10. Simulation results.

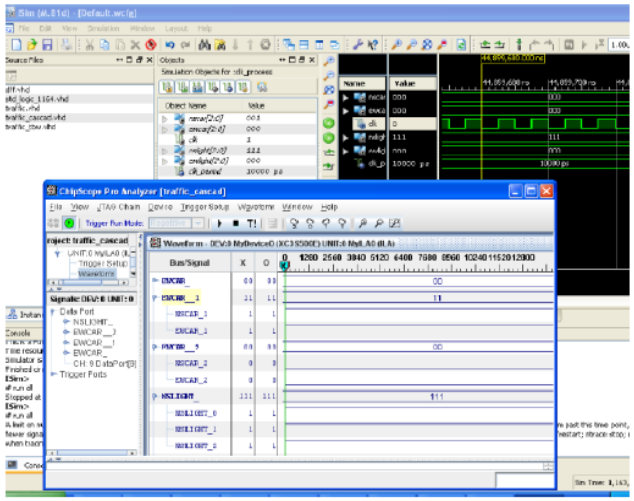

Fig.11. Comparison of Chip scope Pro with behavioral simulation results.

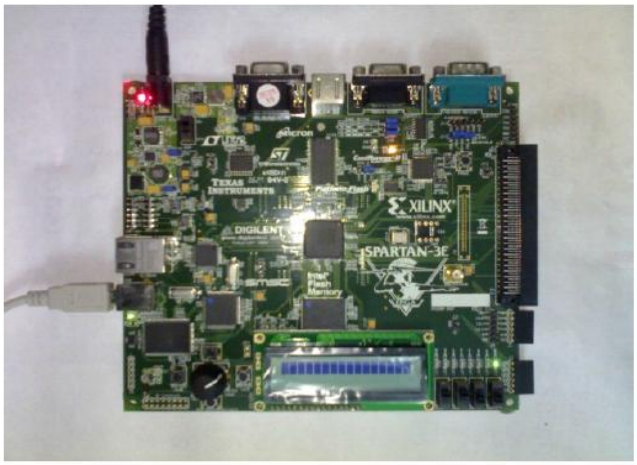

Fig.12. Implementing on an FPGA kit.

```
Entity traffic_cascad is
Port (nscar, ewcar: in STD_LOGIC_VECTOR (2
Downto 0);
Clk: in STD_LOGIC;
Nslight, ewlight: out
STD_LOGIC_VECTOR (2 downto 0));
End traffic_cascad;
```

Fig.13. Structure of the entity.

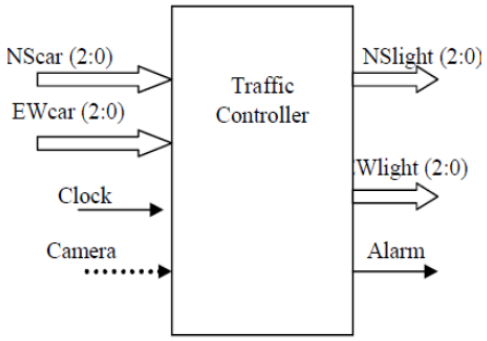

Fig.14. The model of the controller.

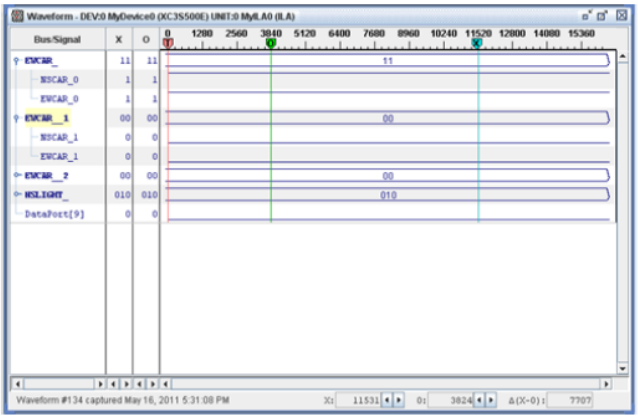

Fig.15. Chips cope verification with 1 Hz frequency.

The in circuit verification has been done with the chips cope pro tool with the help of which real time signal flow has been detected and verified with the theoretical results [5]. The total number of samples taken for testing is 16384. So from there we can calculate the time taken for an arbitrary number of samples. The Spartan 3E board produces a clock sampling rate of 50 MHz and from there we have converted the clock to 1 Hz so that when both NS car and EW car are present at a particular junction the NS light and EW light alternatively glows for the specific time period set by us according to the frequency. The pseudo code is as shown below.

Pseudo-code:

Process (clk) /* clock process

Variable clk_cnt: integer from 0 to 49999999

```
Begin

If rising_edge (clk) then

Clk_cnt++;

If clk_cnt=49999999 then

clk_1hz<='1';

Else

clk_1hz<='0';

End if;

End if;

End process;
```

V. CONCLUSION

This design uses the VHDL hardware language description by text. In the establishment of the general expectation function, it uses the hierarchical design to realize alternating lit the traffic lights, the countdown time display and vehicles' and pedestrians' safe passing command. The program's data can be set base on actual conditions (flexible modification). In the future, we will further improve the function of some modules, such as FPGA/CPLD kit validation.

VI. REFERENCES

[1] Sourav Nath, Chandrajit Pal, Suman Sau, Sreyanka Mukherjee, Abhishek Roy, Arghya Guchhait and Debdatta Kandar, "Design of an FPGA Based Intelligence Traffic Light Controller with VHDL", December, 2012. Pp.92-97.
[2] Traffic light, Wikipedia the free encyclopedia.
[3] FPGA-Based Advanced Real Traffic Light Controller System Design WM El-Medany, MR Hussain.
[4] www.cs.fsu.edu/~zzhang/CDA3100_Spring_2011_files/ week11_1.ppt.
[5] ChipscopePro, ISE 10.1 and Xilinx Simulator on the Digilent Spartan-3E board.
[6] Design of an Intelligence Traffic Light Controller (ITLC) with VHDL Taehee Hm, Chiho Lin (Dept. of Computer Science, Semyung University).
[7] Xpower estimator user guide (ug440). www.xilinx.com/ power.
[8] http://www.xilinx.com/itp/xilinx10/isehelp/ise_p_viewing _a_technology_schematic_xst.htm.
[9] Design of FPGA-Based Traffic Light Controller System M.F.M.Sabri, M.H.Husin, W.A.W.Z.Abidin, K.M.Tay, H.M.Basri, Dept. of Electronic Engineering, Faculty of Engineering, University Malaysia Sarawak, Sarawak, Malaysia msmfaizrizwan@feng.unimas.my, 978-1-4244-8728-8/11.
[10] Design and Implementation of FPGA-Based Adaptive Dynamic Traffic Light Controller Shwetank Singh, Shailendra C. Badwaik ,Dept. of Electronics & Tele-communication, Sinhgad College of Engineering Pune, India,sshwetanksingh17@gmail.com,scbadwaik.scoe@sinhg ad. edu.
[11] FPGA-Based Advanced Real Traffic Light Controller System Design WM El-Medany 1, MR Hussain 2 CE Department, IT College, UOB, 32038 Bahrain melmedany@itc.uob.bh, http://people.man.ac.uk/~mbgedwme/ GEOMATEC, Spatial Information Research, Manama, Bahrain, marwan@ geomatec.com.
[12] FPGA-Based Dual-Mode Traffic Lights System Design, Liu Zhenggang Xiong Jialong Zhou Mingyun Instructors Yang Jun Ding Hongwei School of Information Science and Engineering, Yunnan University Kunming, China,junyang @ynu.edu.cn.