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Design of Novel 4-Bit Multiplier Circuit by using Self Resetting Modified GDI Logic (SR-MGDIL)

SREENIVASULU PASUPULETI[1], C. PAKKIRAIAH[2]
[1]Research Scholar, Dept of ECE, Annamacharya Institute of Technology & Sciences, Andhrapradesh, India,
Email: psreenivasulu723@gmail.com.
[2]Assistant Professor, Dept of ECE, Annamacharya Institute of Technology & Sciences, Andhrapradesh, India,
Email: cpakkiraiah1988@gmail.com.

Abstract: The multiplier is one of the basic functions used in various VLSI applications. The primary issues in the design of multiplier cell are area, delay and power dissipation. Optimization of several devices for speed and power is a significant issue in low-voltage and low-power applications. These issues can be overcome by incorporating Gated Diffusion Input (GDI) technique. Different types of multipliers are available in the previous depending upon the requirements and various companies are using different types of multipliers according to their needs. In this paper we used new 4 bit multiplier.Gate Diffusion Input (GDI) with level restoration has the conductance overlap between NMOS and PMOS devices so providing high short circuit power dissipation and providing low Output Voltage VoH. Further to reduce the number of transistors and power in SRL-GDI based full adder, the self-resetting logic with modified gate diffusion input logic (SRL-MGDI) is proposed to achieve the low area, low power and high speed. Comparison between SRL-GDI and SRL-MGDI is performed to analysis the circuit functionality in precharge and evaluate paths. The circuit is designed by using tanner toolv13.0.

Keywords: Self-Resetting Logic, Gate Diffusion Inputtechnique, Dynamic Logic, Full Adders.

I. INTRODUCTION

VLSI is one of the most modern developments in IC integration. They include more than 10000 transistors per chip. They cannot be operated by normal programming and have specialized programming and coding techniques. Also they paved the way for ASIC designs, VLSI design flows and complex integrated circuits. They helped in revolutionizing the IC technology. Very large scale-integration (VLSI) is the process of creating an integrated circuit by combining thousands of transistors into a single chip. VLSI began in the 1970 when complex semiconductors and communication technologies have been developed. The microprocessor is a VLSI device. Before the introduction of VLSI technology most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI lets IC makers add all of these into one chip. There are certain key issues that serve as active areas of research and are constantly improving as the field continues to mature. The figures would easily show how Gordon Moore proved to be a visionary while the trend predicted by his law still continues to hold with little deviations and don’t show any signs of stopping in the near future. VLSI has come a far distance from the time when the chips were truly hand crafted. But as we near the limit of miniaturization of Silicon wafers, design issues have cropped up. VLSI is dominated by the CMOS technology and much like other logic families, this too has its limitations which have been battled and improved upon since years.

Taking the example of a processor, the process technology has rapidly shrunk from 180 nm in 1999 to 60nm in 2008 and now it stands at 45nm and attempts being made to reduce it further (32nm) while the Die area which had shrunk initially now is increasing owing to the added benefits of greater packing density and a larger feature size which would mean more number of transistors on a chip. With continual technology scaling improvement in integrated systems has becomes faster and thus it is employed in real time applications in mobile communications, signal processing applications and image processing ect., In every processing applications has the major component called CPU with ALU. Every ALU defines the communication speed of the process, every ALU has number of multipliers, and every multiplier has number of adders and every Adder has number of logic gates and each logic gate has number of MOS Transistors. When we reduce the number of transistor in the logic gate, the parameter such as speed of the process will get increase due to its less delay because of its less complexity. Because of less complexity the area gets reduced. So that the cost of the system also reduces. SRL Logic is used to restore the value capability. The GDI (Morgenshtein et al., 2002; Uma and Dhavachelvan., 2012b; Agrawal et al., 2009) is the lowest power design technique, which is suitable for designing fast, low-power circuits, using reduced number of transistors (as compared to Transmission Gate and CMOS).

The main drawbacks associated with GDI include: The bulk terminals are not properly biased thereby the circuit exhibits threshold drop and variation in Vt. Because of floating bulk, the cells can be implemented in SOI process which would increase the cost of the fabrication. These demerits can be overcome by permanently connecting the bulk terminals pMOS to VDD and nMOS to GND which resolves the threshold variation. This configuration provides suitability for fabricating the logic cells in CMOS p-well and n-well process. Until today static CMOS has been the design style of choice for IC designers due to its robustness against voltage scaling and transistor sizing (high noise margins) and thus the operation is reliable at low voltages (Bisdounis et al., 1998). The disadvantage of CMOS is the substantial number of large pMOS transistors, resulting in high input loads and when the operating frequency increases the circuit dissipates more power. The propagation delay is slightly higher when compared to other logic family due to its larger node capacitances. Dynamic logic families are a good candidate for high speed and high performance circuit than the conventional static CMOS. Dynamic logic requires fewer transistors to implement a given logic function, less area and fasterswitching speed due to its reduced load capacitance (Yee and Sechen, 1996; Balsara and Steiss., 1996; Srivastava et al., 1998. However this circuit suffers from charge sharing, charge leakage, loss of noise immunity, timing problem due to clock input and feed through.

II. INTRODUCTION TO MGDI LOGIC

Among the forceful investigation in the field of low power, high speed digital applications due to the growing demand of systems like phones, laptop, palmtop computers, cellular phones, wireless modems and portable multimedia applications etc has directed the VLSI technology to scale down to nano-regimes, allowing additional functionality to be incorporated on a single chip. The designer‟s novel purpose in the field of multifaceted digital circuit design is minimization of power consumption. These investigations are responsible for special design techniques for digital circuits distant from conventional CMOS design style. A large body of investigate has been performed to expand and advance conventional Complementary Metal Oxide Semiconductor (CMOS) techniques for the fabrication of ULTRA low power integrated circuits (ICs). The purpose of this study is to expand a faster, lower power, and reduced area substitute to standard CMOS logic circuits. Mod-GDI technique is one such new technique for minimization of power consumption in the digital circuit design field.

III. SELF RESETTING LOGIC WITH GATE DIFFUSION INPUT (SRLGDI)

Self-resetting circuitry automatically precharges themselves (i.e., reset themselves) after a prescribed delay by conditionally charging the dynamic nodes to evaluate the desired logic function using a local feedback timing chain instead of a global clock. Although this SRCMOS logic inherits lot of merits, it still suffers from static power dissipation due to the nMOS logic structure. As stated earlier, during precharge the nMOS stack is completely open and the output is fed back to the pMOS block to charge the capacitor Cy. During this period the nMOS transistors operate in cut-off region exhibiting subthreshold current. Moreover during the evaluation phase when the entire nMOS transistor in the n-block and Preset transistor is ON direct impedance path exists between the VDD of Preset transistor and nMOS block leading to static power dissipation. The width of the pulses must be controlled carefully or else there may be contention between nMOS and pMOS devices, or even worst, oscillations may occur. These demerits can be surmounted using GDI technique. The change done in the existing SRCMOS, instead of nMOS logic pull down tree, it is replaced by GDI logic with level restoration.

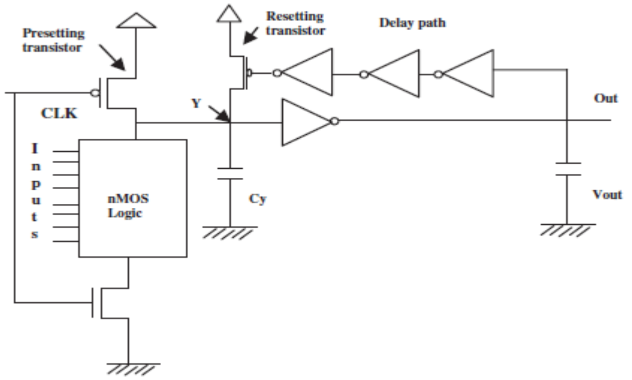


Fig 1. Self reseting logic for CMOS

A. Operation of Srlgdi Logic

The general behaviour of SRLGDI logic can be portrayed as an ability of a logic block to reset its output pulse after it has been asserted. The reset signal is often generated within the block based on the output pulse. The circuit operation is defined in two phases as precharge and evaluation. The switching behaviour is elucidated in Fig. 5, where Ppreset and Preset define the pMOS precharge and reset transistor. During the precharge phase CLK= 0 in Fig. 5a, the GDI block is open, the transistor Ppreset is ON so a direct impedance path exists between node y and VDD thereby charging the capacitance Cy to VDD. The output node Vout is discharged and makes the reset voltage Vreset to be '0' insuring that Preset is cut-off during this time. For the evaluation phase CLK= 1 as shown in Fig. 5b, the GDI logic is closed, the transistor Ppreset is OFF, in this case Vy fi 0 V and the output capacitance charges to give an output voltage Vout fi VDD. This voltage is fed through the delay path and produces Vreset fi VDD and the transistor Preset is active after the specified delay path. The Preset transistor recharges the node capacitor Cy back up to a voltage of Vy fi VDD.

This action resets the output voltage to its original precharge value of Vout fi 0 V. Basic SRLGDI logic gates (AND, OR, NAND, NOR, XOR,and XNOR) are shown in Fig.2. Each gate consists of a GDIlogic tree, half-latch circuits, Preset device, and a diagnostic(static_evaluate) weak pMOS (Preset) device. The GDI tree isa parallel/series network of nMOS and pMOS devices betweenground and the inputs to the output inverters (the dynamicstorage nodes). The GDI network is incorporated with levelrestoration circuit for full swing output. The delay path is limitedwith one inverter in order to have smaller pulse width toavoid the contention problem between the GDI network and the dynamic nodes. This structure produces equal fall and risedelay. The delay line should be implemented with odd numberof inverters in order to ensure the correct transition (ON andOFF) for Preset transistor charging and discharging thedynamic capacitor Cy. The inverter at the output nodeproduces both true and complementary outputs.

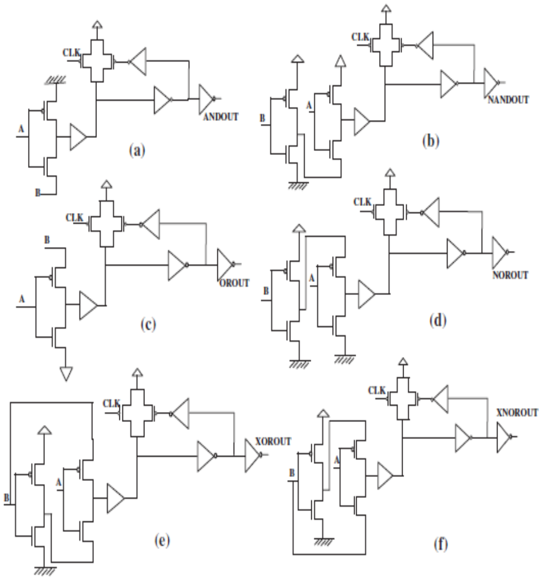
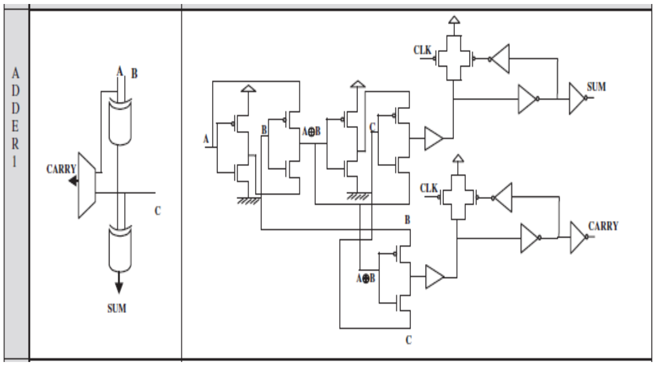


Fig 2. 2-Input primitive cells in Self Resetting Logic with gate diffusion input level restoration buffer. (a) AND gate, (b) NAND gate, (c)OR gate, (d) NOR gate, (e) XOR gate and (f) XNOR gate.

Addition is an indispensable operation for any high speed digitalsystem, digital signal processing or control system. The primaryissues in the design of adder cell are area, delay andpower dissipation. The proposedadder circuit realizations are shown in Fig . Adder1 is implementedwith XOR and multiplexer. The sum logic is evaluatedby XOR gate and carry logic is realized using MUX. Adder2 isdesigned using XNOR and MUX with sum realization usingXNOR and MUX, while carry logic is structured using MUX. Adder3 is proposed with XNOR and MUX with sumevaluation using XNOR and carry using MUX. To test theperformance of the proposed and existing adders, detailedcomparisons were performed. The simulations were run withthe tanner software.



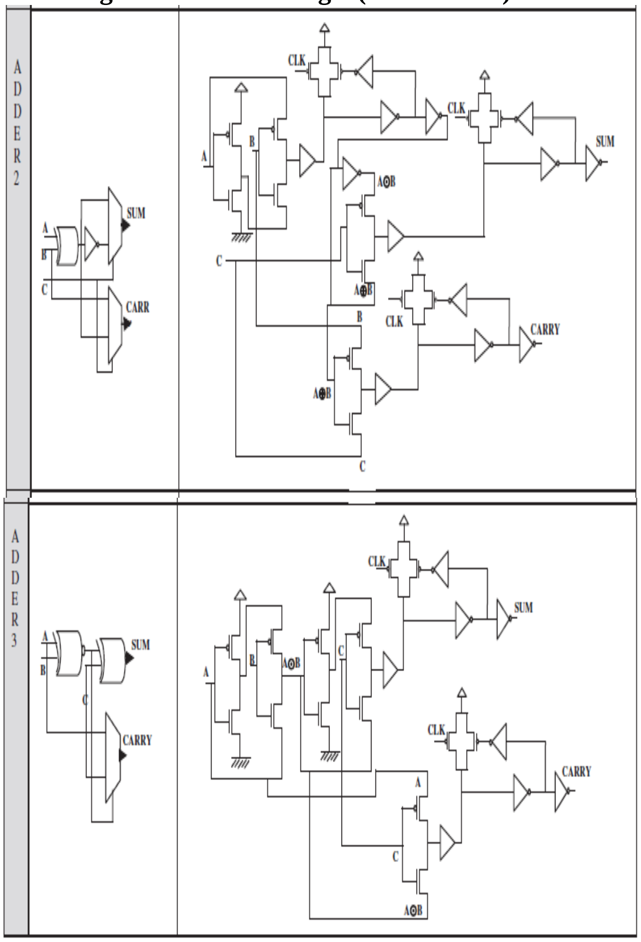


Fig 3. full adders.

IV. PROPOSED SELF RESETTING LOGIC WITH MODIFIED GATE DIFFUSION INPUT (SRL-MGDI)

In SRL-MGDI xor gate to design withonly three transistors. The design is shown below figure and similarly to design half adder and full adder by using three transistors xor gates.

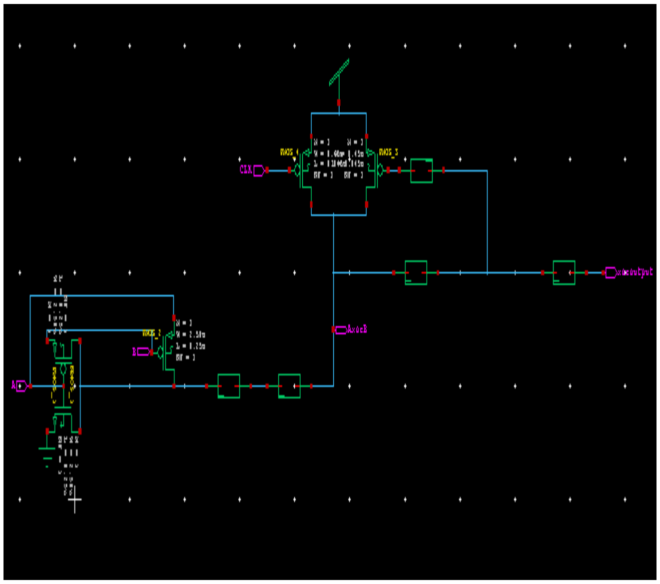


Fig 4. Xor gate with three transistors.

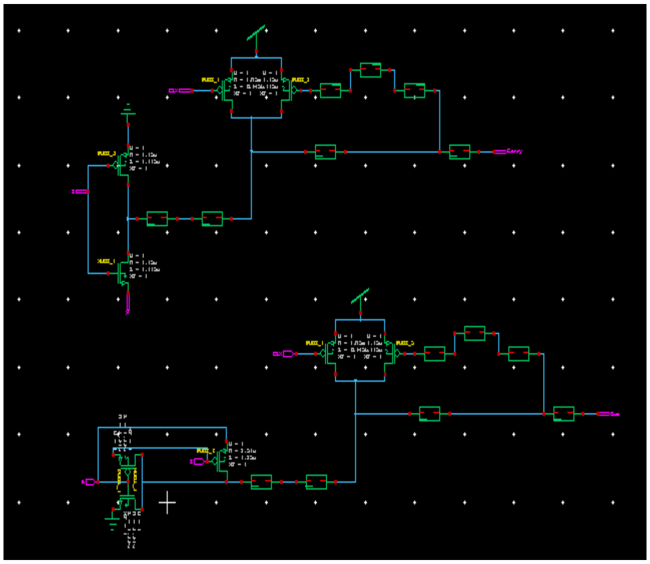


Fig 5. Half adder with three transistors xor gate

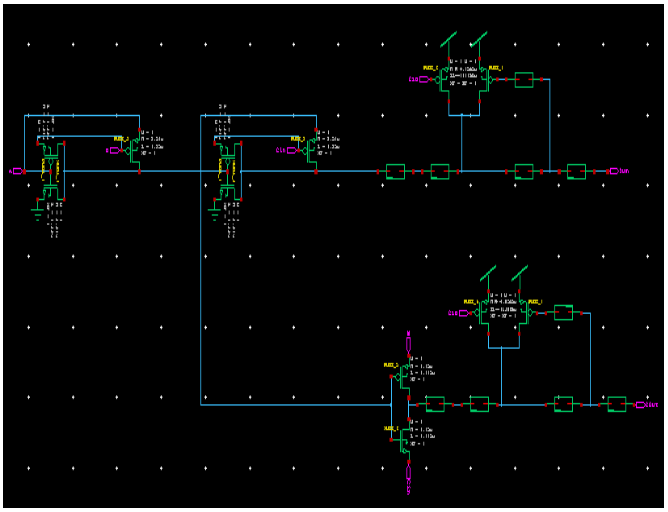


Fig 6. Full adder with three transistors xor gate.

V. RESULTS

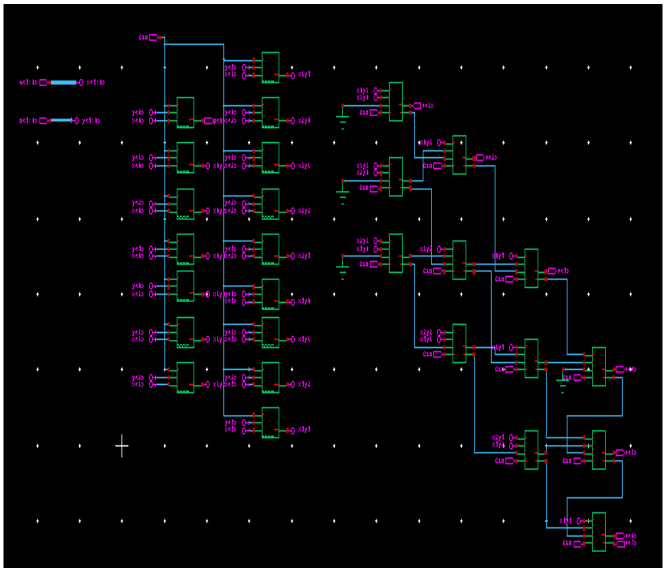


Fig7. 4-bit multiplier by using SRL-MGDI.

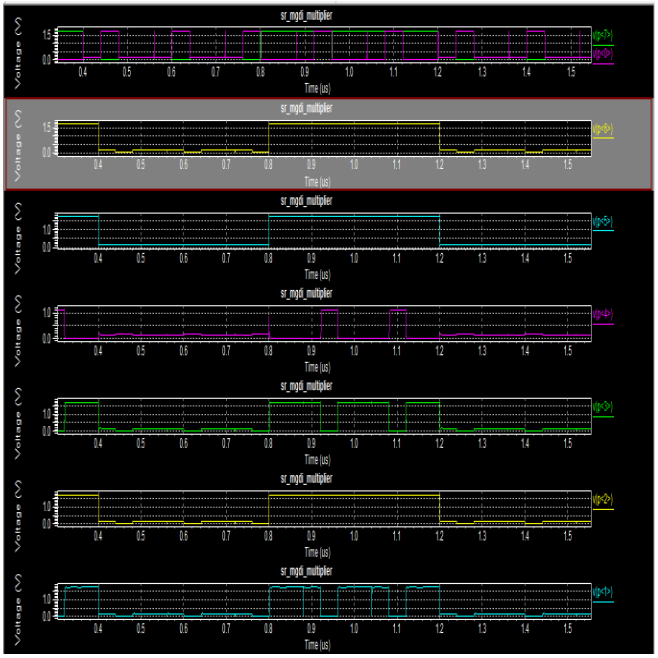


Fig8. Simulation Results.

Table1: Comparision of SRL-GDI and SRL-MGDI

Parameters	SRL-GDI	SRL-MGDI
Area	632	608
Power(mW)	96.57	94.37
Delay(ns)	0.14	0.53

Number of Transistors:

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Device and node counts:
           MOSFETs - 608                    MOSFET geometries - 8
              BJTs - 0                                  JFETs - 0
           MESFETs - 0                                 Diodes - 0
        Capacitors - 0                              Resistors - 0
         Inductors - 0                       Mutual inductors - 0
 Transmission lines - 0           Coupled transmission lines - 0
    Voltage sources - 10                     Current sources - 0
              VCVS - 0                                   VCCS - 0
              CCVS - 0                                   CCCS - 0
  V-control switch - 0                      I-control switch - 0
     Macro devices - 0            External C model instances - 0
       HDL devices - 0
       Subcircuits - 0                   Subcircuit instances - 228
 Independent nodes - 2684                      Boundary nodes - 11
       Total nodes - 2695
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VI. CONCLUSION

The proposed SRL_MGDI primitives are simulated using Tanner EDA with BSIM 45nm lm technology with supply voltage ranging from 0 V to 5 V in steps of 0.2 V. All the primitive gates are simulated with same setup. The test bed is supplied with a nominal voltage of 5 V in steps of 0.2 V and it is invoked with the technology library file Generic 025. To establish an unbiased testing environment, the simulations have been carried out using a comprehensive input signal pattern, which covers every possible transition for a logic gate. All the primitive structures are implemented in CMOS, Dynamic logic (DY), SRCMOS and SRLMGDI with the same set up, providing the same temperature, biasing, aspect ratio and testing condition. All transitions from one input combination to another have been tested, and the delay at each transition has been measured. The average has been reported as the cell delay. The power consumption is also measured for these input patterns and its average power is reported with otherlogic like CMOS, GDI, SRCMOS and Dynamic logic.

VII. REFERENCES

[1] A. Morgenshtein, A. Fish, I.A. Wagner, ”Gate-Diffusion Input (GDI)- A Power Efficient Method for Digital combinatorial circuits”, IEEE Transactions on VLSI Systems,vol.10, no.5, October 2002.

[2] A. Morgenshtein, I. Shwartz, A. Fish, ”Gate Diffusion Input (GDI) Logic in Standard CMOS Nanoscale Process”, 2010 IEEE 26th Convention of Electrical and Engineers in Israel.

[3] S. Fisher, A. Teman, D. Vaysman, A. Gertsman, O.Y.Pecht, A. Fish, ”Ultra-Low Power Subthreshold Flip-Flop Design”, IEEE International Symposium on Circuits and Systems (ISCAS), 2009.

[4] K.Roy, S.Prasad, ”Low-Power CMOS VLSI Circuit Design”,Wiley India 2009.

[5] Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic; Reto Zimmermann and Wolfgang Fichtner, Fellow, IEEE; IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 32, NO. 7, JULY 1997.

[6] Design Technologies for Low Power VLSI; Massoud Pedram;Department of EE-SystemsUniversity of Southern California Los Angeles , CA 90089; Encyclopedia of Computer Science and Technology, 1995.

[7] Low Power Digital design using modified GDI method;Padmanabhan Balasubramanian and Johince John,2006, IEEE.

[8] ASIC primitive cells in Modified Gate Diffusion Input Technoque; R.Uma and Dhavachelvan;pp. 467- 474,springer India,2013.

[9] Basic Low Power Digital Design; P.R. Panda et al., Power-efficient System Design, DOI 10.1007/978-1-4419-6388-82,Springer Science+Business Media, LLC 2010.

[10] Minimizing Power Consumption in Digital CMOS circuits,ANANTHA P. CHANDRAKASAN AND ROBERT W. BRODERSEN, FELLOW, proceedings of IEEE, Vol. 83 No. 4, April 1995.

Authors Profile:

Sreenivasulu Pasupuleti, Received B.tech Degree in (ECE). Currently he is Doing M.tech (VLSI Design) in Annamacharya Institute of technololgy and science, Tirupati. His General Area of Interest is Digital design, Verilog HDL, RTL Design, System Verilog, VLSI Testing and Verification.

C.Pakkiraiah,have over 4+years’ experience in Teaching with reputed Engineering colleges. Currently working with Annamacharya Institute of Technology and science, as assistant professor. His research areas are Low Power VLSI, Digital IC Design, Signal processing, image processing and communications systems.