International Journal of VLSI System Design and Communication Systems

ISSN 2322-0929
Vol.03, Issue.04,
July-2015,
Pages:0445-0447

www.ijvdcs.org

A Fast Binary to BCD Conversion for Binary/Decimal Multi-Operand Adder

M. SHIRISHA[1], M. CHANDRASHEKHAR[2]

[1]PG Scholar, Ganapathi Engineering College, Rangshaipeta, Warangal, TS, India.
[2]Assistant Professor, Ganapathi Engineering College, Rangshaipeta, Warangal, TS, India.

Abstract: This paper presents a new architecture for a Binary to BCD (BD) converter which forms the core of our Proposed high speed decimal Multi-operand Adder. Our proposed design contains various improvements over existing architectures. These include an improved BD Converter that helps in reducing the delay of the Multi-operand decimal Adder. Simulation results indicate that with a marginal increase in area, the proposed BD converter exhibits an improvement of 82% in delay over earlier designs. Further the decimal Multi-operand Adder achieves faster design when compared to previously published results.

Keywords: Decimal Arithmetic, Binary to BCD Converter, Multi-Operand Adder.

I. INTRODUCTION

The use of decimal arithmetic has been increasing over binary due to increase in the applications of internet banking and there are many others places where precision is very important. Binary digits have a disadvantage of not being able to represent digits like 0.1 or 0.7, requires an infinitely recurring binary number. The availability of multi-operand decimal adders can facilitate financial and commercial applications based on existing huge databases. The simultaneous addition of several decimal numbers is the common operation in multiplication and division algorithms. Multi-operand addition is a vital operation as it is a core component of arithmetic operations, such as division and multiplication. In case of decimal multiplication Multi-operand decimal addition comes in handy for swiftly summing large amounts of decimal data. This paper introduces a multi-operand decimal addition algorithm by employing high speed binary to BCD converter circuit, which speeds up the process of decimal addition when multiple BCD operands are added together. A Novel design for binary to BCD converter circuit is proposed. Further, analysis is done with respect to the existing binary to BCD converter architectures.

The proposed algorithm is fundamentally different from multi-operand BCD addition algorithms[3,5] since intermediate BCD corrections are not done rather correction is done at the final stage to get proper BCD results. As the decimal corrections are achieved separately from the computation of the binary sum, such that the layout of the binary carry-save adder does not require any further rearrangement, the design can perform as unified Binary/ BCD multi-operand adder. In the next section, we present preliminary information about the previous work on multi-operand adders and discuss the binary to BCD converter. The proposed design is presented in section III. Experimental results related to the performance of existing and proposed multi-operand adders are compared in section IV and conclusions are drawn in section V.

II. EXISTING SYSTEM

A. Block Diagram

Block diagram is as shown in Fig.1.

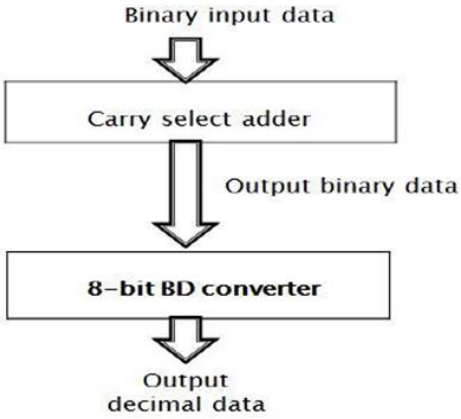

Fig.1. Block diagram.

B. Carry Select Adder

In Present generation in VLSI system are more concentrating in the reduction of area and power and increasing the speed of operation of the circuit. The carry select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two RCA. One time with assumption of carry input as 0 and another time with carry as 1.After the results are calculated, the final sum and the final carry is selected is selected with the multiplexer by the previously generated carry out. The speed in the SQRT CSLA is dependent on the carry generation of the previous cascaded RCA. The sum of the each bit is generated sequentially one after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many

electronic applications to alleviate the problem of carry propagation delay by independently generating the multiple carries and then select the carry to generate the sum. However, the CSLA is not area efficient because it contains multiple Paris of cascaded RCA with input C_{in}=0 and C_{in}=1, to generate partial sum and carry, then the final sum and carry are selected by multiplexers.

The CSA is used in many computational systems design to moderate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. It uses independent ripple carry adders (for C_{in}=0 and C_{in}=1) to generate the resultant sum. However, the Regular CSA is not area and speed efficient because it uses multiple pairs of Carry select Adders to generate partial sum and carry by considering carry input. The final sum and carry are selected by the multiplexers. A carry-select adder is divided into sectors, each of which – except for the least-significant – performs two additions in parallel, one assuming a carry-in of zero, the other a carry-in of one. A four bit carry select adder generally consists of two ripple carry adders and a multiplexer. The carry-select adder is simple but rather fast, having a gate level depth. Adding two n-bit numbers with a carry select adder is done with two adders (two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known. The design schematic of Carry Select Adder is shown in Fig.2. A carry-select adder speeds 40% to 90%faster than RCA by performing additions in parallel and reducing the maximum carry path.

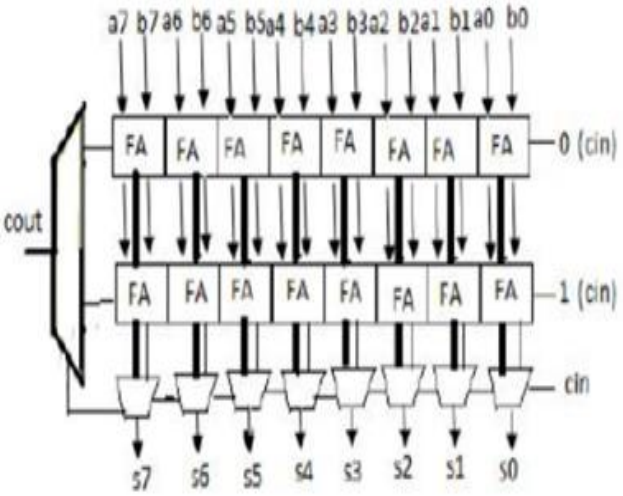

Fig.2. Carry select adder.

The conversion of the obtained sum from the carry select adder is given onto the shift and add three converter, using which we can attain a BCD.

III. PROPOSED SYSTEM

A. Block Diagram

Block diagram is as shown in Fig.3.

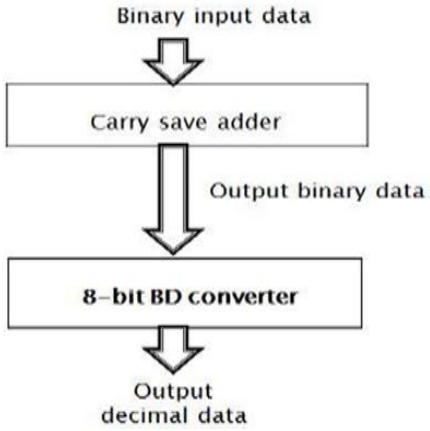

Fig.3. Proposed design block diagram.

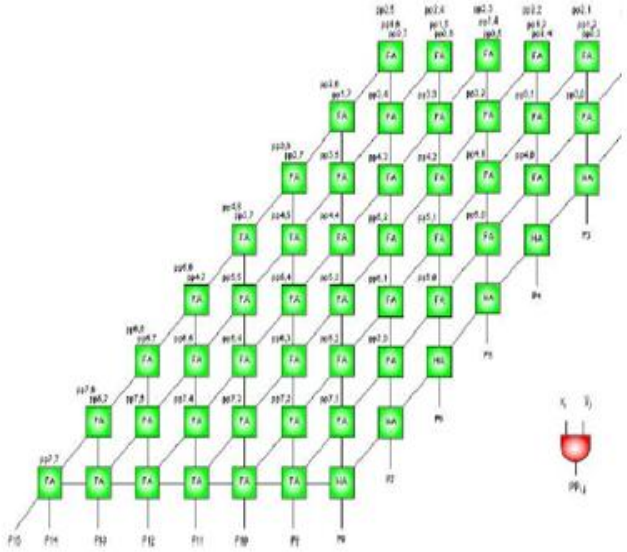

Fig.4. Carry save adder.

B. Carry Save Adder

There are many cases where it is desired to add more than two numbers together. The straightforward way of adding together m numbers (all n bits wide) is to add the first two, then add that sum to the next, and so on. This requires a total of m − 1 additions, for a total gate delay (assuming look ahead carry adders). Instead, a tree of adders can be formed, taking only gate delays. Using carry save addition, the delay can be reduced further still. The idea is to take 3 numbers that we want to add together, x + y + z, and convert it into 2 numbers c + s such that x + y + z = c + s, and do this in one time. The reason why addition cannot be performed in one time is because the carry information must be propagated. In carry save addition, we refrain from directly passing on the carry information until the very last step. We will first illustrate the general concept with a base 10 example. To add three numbers by hand, we typically align the three operands, and then proceed column by column in the same fashion that we perform addition with two numbers as shown in Fig.4. The three digits in a row are added, and any overflow goes into the next column. Observe that when there is some non-zero carry, we are really adding four digits (the digits of x,y and z, plus the carry).

C. BD Converter

In the proposed binary to decimal converter for conversion process we use shift and add 3 algorithm. Steps used in algorithm:

- Shift the binary number left one bit.
- If 8 shifts have taken place, the BCD number is in the Hundreds, Tens, and Units column.
- If the binary value in any of the BCD columns is 5 or greater, add 3 to that value in that BCD column.
- Repeat the above process.

IV. SIMULATION RESULTS

Simulation results of this paper is as shown in Fig.5.

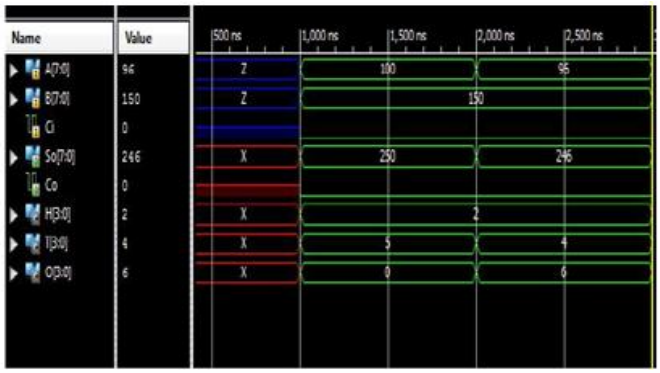

Fig.5. Simulation results for proposed system.

TABLE I: Synthesis Report

Parameter	Carry select adder with converter	Carry save adder with converter
Delay	10.5 ns	8.6ns
Area (slices+LUTs)	31	33

V. CONCLUSION

In this proposed approach, which includes a carry save adder and binary to BCD converter gets a better result compared to the existing design and simulation results shows the delay variations which is a key advantage. In the proposed system the delay is decreased to 80% when compared to existing design.

VI. REFERENCES

[1] M. F. Cowlishaw. Decimal floating-point: Algorism for computers. In Proc. IEEE 16th Symposium on Computer Arithmetic, pages 104–111, July 2003.

[2] M. D. Ercegovac and T. Lang, Digital Computer Arithmetic. Elsevier/Morgan Kaufmann Publishers, 2004.

[3] R. D. Kenney and M. J. Schulte. High-speed multi-operand decimal adders. IEEE Trans. on Computers, 54(8):953–963, Aug. 2005.

[4] Dadda, Luigi. "Multi-operand parallel decimal adder: A mixed binary and bcd approach." Computers, IEEE Transactions on 56.10 (2007): 1320-1328.

[5] Lin, Kuan Jen, et al. "A parallel decimal adder with carry correction during binary accumulation." New Circuits and SystemsConference(NEWCAS),2012IEEE10th International. IEEE, 2012.

[6]- Jaberipur, Ghassem, and Amir Kaivani. "Improving the speed of parallel decimal multiplication." Computers, IEEE Transactions on 58.11 (2009): 1539-1552.

[7]- Bhattacharya, Jairaj, Aman Gupta, and Anshul Singh. "A high performance binary to BCD converter for decimal multiplication." VLSI Design Automation and Test (VLSI-DAT), 2010 International Symposium on. IEEE, 2010.

[8]- Al-Khaleel, Osama, et al. "Fast and compact binary-to-BCD conversion circuits for decimal multiplication." Computer Design (ICCD), 2011 IEEE 29th International Conference on. IEEE, 2011.

[9] S. Knowles, ‘‘A family of adders,’’ in: Proceedings of the 14th IEEE Symposium on Computer Arithmetic, pp. 30–34, 1999.

Author’s Profile:

Ms. M. Shirisha pursuing her M.Tech specialized in VLSI in Ganapathi College of Engineering, Rangshaipet, Warangal, Telengana. She completed her B. Tech in Electronics and Communication Engineering and intrested to research work in VLSI.

Mr. Mothukuri Chandrashekar working as Assistant Professor in Ganapathi College of Engineering in ECE Dept. He has completed his M.tech and B.tech and is interested in the area of VLSI.