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Design of Fuzzy Inference Processor-A MAX-MIN Calculator Circuit for MMF

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Abstract: The fuzzy logic is effectively connected in different applications in all fields of engineering and science including buyer gadgets, control systems, signal and image processing etc.The different fuzzy processing systems have been utilized by distinctive specialists for advancement of different applications. The focal point of fuzzy systems is to approximate system behavior where numerical relations don't exist. The fundamental point of fuzzy logic system is to create an impersonation of a human sagacious system, with the capacity of controlling a given application without any mathematical model. A given a set of input data, the fuzzy inference processor estimate the proposed activities as indicated by their conformance with the knowledge base. A real-time fuzzy inference involves processing the knowledge base within constant period of time and with minimum speed of one MFLIPS (Mega fuzzy logic inferences per second). The drawback of high latency of matching degree(MD) calculation between the fuzzified input and the antecedent membership functions (MF) is addressed by implementing a multi membership function (MMF) based MAX-MIN calculator circuit to improve the fuzzy inference for the first time in comparison to the existing architectures of MAX-MIN circuits which deal with just one MF at a time. The proposed architecture calculates the matching degree of trapezoid triangular and gaussian together. The architecture is modeled in VHDL and implemented in XILINX and Spartan field programmable gate arrays (FPGA).

Keywords: Fuzzy Inference Processor, Matching Degree, Membership Function, FPGA.

I. INTRODUCTION

Presently a-days control systems has got need in different applications; a control system is one which control activity relies on upon one of the parameter in framework and it needs numerical estimations for control activity, these numerical models are erroneous and the improvement of applications using software languages is intense. Here we utilize a model which can control without any use of numerical values called fuzzy logic. The thought of fuzzy logic was proposed in the paper by Lotifi A Zadeh of the University of California at Berkeley in 1965. He uses computing with numbers to computing with words.Fuzzy logic replaces all conventional control systems. Because of the advantages more scientists are going to utilize in numerous applications. The digital hardware fuzzy inference processor was originally developed by Togai and Watanabe et al. Many variations have been proposed to improve the inferencing performance. Asica, Catania and Russo et. al assume that every membership function is composed of nine segments. They use a binary search algorithm to calculate the matching degree between two membership functions.

The inference speed of their fuzzy inference processor depends on the number of active rules. Shih-hsu huang and jian-yuan lai et. al assumes that each membership function is composed of four segments and 64 rules with fuzzified inputs at a speed of 7 MFLIPS. Loan, S.A. and A. M. Murshid et. al assumes that each membership function composed of three segments and 64 active rules but it requires more area compared to Loan, S.A. and A. M. Murshid et. al with four segments and 64 rules. In my proposed design assume that each membership function composed of five segments,64 rules and it work for three membership functions: triangular and trapezoidal and Gaussian together. Because of combined architecture of Loan, S.A. and A. M. Murshid et. al and et. al and pipelining, usage of LUTs and slice latches are reduced.

II. THE FUZZY LOGIC SYSTEM

The conventional fuzzy system consists of three blocks as shown in Fig.1. The operation of Fuzzy Logic system is explained as follows; firstly a crisp set of input data is converted into a fuzzy set using fuzzy linguistic variables

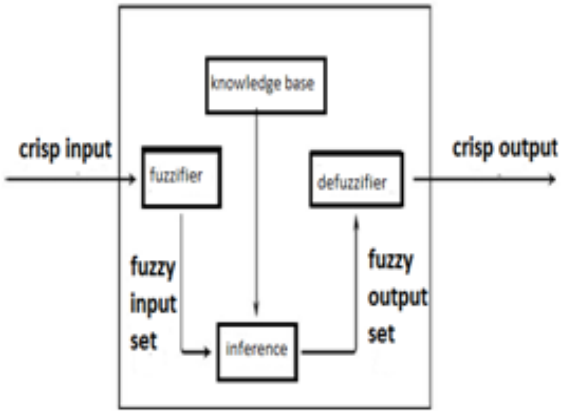

Fig.1. Fuzzy Logic System.

and membership functions. This step is called as fuzzification. Inference system consists of set of rules which maps the fuzzified membership functions into set of output membership functions. Finally the defuzzifier converts the output membership functions into crisp output. The inference engine performance, particularly the processing speed, is an important measure in case of inference engine. The speed limitation of the inference engine lies in the calculation of the matching degree between the fuzzified input and the antecedent membership functions.

III. MAX–MIN CALUCLATOR CIRCUIT

The calculation of matching degree (MD) between the fuzzified input and the antecedent MF's is an important parameter. In this work, a new multi membership function (MMF) MAX-MIN calculator is being proposed, calculating the MD between the three types of MF's, Triangular, Trapezoid and Gaussian together. Assume a general antecedent five point MF" A(a1,a2,a3,a4 and a5)" and a five point fuzzified input MF " X(x1,x2,x3,x4 and x5)".Since Gaussian, Trapezoid and Triangular MF's use 5,4 and 3 points respectively, these MF's can be extracted from the general antecedent and the fuzzified MFs.

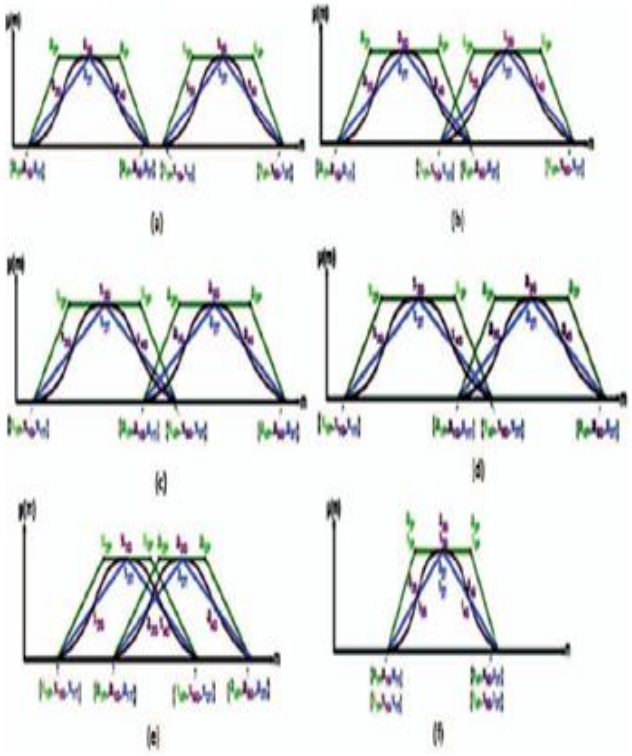

Fig.2. Different states of the various MMFs (a) no matching (b), (c), (d) and (e) cross-over points (f) complete matching.

Fig.2 shows the different states of the various MFs. Fig.2(a) shows that the MF's are completely mismatched, Fig.2(f) shows that the MF's are completely matched and Fig.2(b-e) shows that the MF's are crossing over each other. The ten mutually exclusive conditions used to compute the MD between the various MF's are given below.

1. If (x5<a1 and x4<a1 and x3<a1) or (a5<x1 and a4<x1 and a3 < x1): MD = '0':Fig. 1(a).
2. If (a4 < x2 and x1 < a5): MD is the grade value of the cross-over point: Fig. 1(b).
3. If (x4 < a2 and a1 < x5): MD is the grade value of the cross-over point: Fig. 1(c).
4. If (x2 ≤ a4 ≤ x3): MD is the grade value of the cross-over point: Fig. 1(d).
5. If (a2 ≤ x4 ≤ a3): MD is the grade value of the cross-over point: Fig. 1(e).
6. If (a3 < x2 and x1 < a4): MD is the grade value of the cross-over point: Fig. 1(b).
7. If (x3 < a2 and a1 < x4: MD is the grade value of the cross-over point: Fig. 1(c).
8. If (a2 < x2 and x1 < a3): MD is the grade value of the cross-over point: Fig. 1(b).
9. If (x2 < a2 and a1 < x3): MD is the grade value of the cross-over point: Fig. 1(c).
10. If (a1=x1 and a2=x2 and a3=x3 and a4=x4 and a5=x5): MD = '1':Fig. 1(f).

To realize efficiently the proposed MMF based MAX-MIN calculator circuit the important step in the algorithm is the comparison of the general antecedent five point MF" A(a1,a2,a3,a4 and a5)" and a five point fuzzified input MF " X(x1,x2,x3,x4 and x5)".

If x5<a1 and x4<a1 and x3<a1 or a5<x1 and a4<x1 and a3<x1, then

$$M.D. = 0^{I}$$

If a4<x2 and x1<a5, then

$$M.D. = 2^{I} - 2^{I}\frac{(x2 - a4)}{(x2 - a4) + (a5 - x1)} \quad (1)$$

If x4<a2 and a1<x5, then

$$M.D. = 2^{I} - 2^{I}\frac{(a2 - x4)}{(a2 - x4) + (x5 - a1)} \quad (2)$$

If x2<a4 and a4<x3, then

$$M.D. = 2^{I} - 2^{I}\frac{(x3 - a3)}{(x3 - a3) + (a4 - x2)} \quad (3)$$

If a2<x4 and x4<a3, then

$$M.D. = 2^{I} - 2^{I}\frac{(a3 - x3)}{(a3 - x3) + (x4 - a2)} \quad (4)$$

If a3<x2 and x1<a4, then

$$M.D. = 2^{I} - 2^{I}\frac{(x2 - a3)}{(x2 - a3) + (a4 - x1)} \quad (5)$$

If x3<a2 and a1<x4, then

$$M.D. = 2^{I} - 2^{I}\frac{(a2 - x3)}{(a2 - x3) + (x4 - a1)} \quad (6)$$

If a2<x2 and x1<a3, then

$$M.D. = 2^{I} - 2^{I}\frac{(x2 - a2)}{(x2 - a2) + (a3 - x1)} \quad (7)$$

If x2<a2 and a1<x3, then

$$M.D. = 2^{l} - 2^{l}\frac{(a2 - x2)}{(a2 - x2) + (x3 - a1)_{l}} \quad \textbf{(8)}$$

If x1=a1 and x2=a2 and x3=a3 and x4=a4 and x5=a5, then

$$M.D. = 1$$

Considering the condition for Eq –[5] for assuming segmented points are aligned as a3 < x2 and x1 < a4

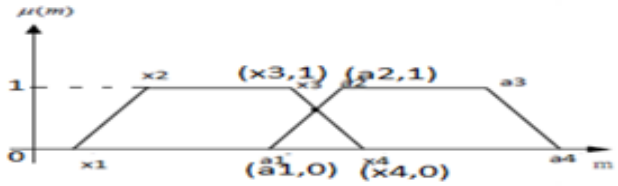

Fig.3.

Equation (9) is obtained from a straight line passing through (x3, 1) and(x4, 0) as

$$\mu(m) = \frac{X - x4}{x3 - x4} \quad \textbf{(9)}$$

Equation (10) is obtained from a straight line passing through (a1, 0) and (a2, 1) as

$$\mu(m) = \frac{X - a1}{a2 - a1} \quad \textbf{(10)}$$

Equating the equations 1a and 1b we get the following equation (11)

$$X = \frac{x4a2 - a1x3}{x4 - x3 + a2 - a1} \quad \textbf{(11)}$$

Substituting the equation 11 into equation 9 or 10 we get matching degree (M.D)

$$\mu(m) = \frac{a2 - x3}{a2 - x3 + x4 - a1} \quad \textbf{(12)}$$

Its discrete equivalent can be obtained by multiplying and subtracting the decimal fraction from the $2^{(segmented\ points)}$.

IV. RESULTS

The proposed architecture of MMF based MAX-MIN circuit has been modeled in VHDL. It is observed that the proposed structure is well optimized in spite handling three MF's together. On comparing the proposed architecture with the architecture developed by S. Huang et al, it is observed that the proposed architecture is area and power efficient. The functional analysis of MMF based MAX-MIN calculator performed and the results in the form of the timing diagram are shown in the fig.4 and shows the magnitude of mismatch between the MF's by the magnitude of cross-over. The input MF's are A(a1,a2,a3,a4,a5) and X(x1,x2,x3,x4,x5). For the values of A(01, 03,05, 07, 09) and X ((01, 03, 05, 07, 09)) are completely matching. The output value of H for this state is 1H, indicating that the all the three MF's are completely matched. Similarly, for the values of A(01, 03, 05 ,07, 09) and X (0A, 0C, 0E, 10, 12) are completely mismatched MF's , the value of H is 0H. These results can be easily checked by taking membership function for ancient and fuzzified input values a1, a2, a3 and x1, x2, x3 are 4, 6, 8 and 1, 3, 5 respectively. The above values are used to compute the matching degree.

Fig.4. Timing diagram of MAX-MIN Calculator.

TABLE I: Device Utilization Summary

	Triangular			Trapezoidal		Gaussian		Proposed MMF		% Saving Resources
Logic Utilization	Availability	Used	Utilization %	Used	Utilization %	Used	Utilization %	Used	Utilization %	Proposed
Number of Slices	768	305	39	325	42	363	47	78	10	92
Number of 4 input LUTs	1536	589	38	642	41	699	45	153	9	92
Number of bonded IOBs	124	40	32	60	48	64	51	89	71	45

This fractional value changed to discrete value by using number of segment points. The above condition comes under the triangular membership function then it uses three segment points for its representation and the graded value made discrete value into 8 levels i.e. matching degree between the values of 0 to 7. For the above condition matching degree (h) obtained as 000000000010. It is shown in simulation result. The comparative analysis is shown in the table. In the proposed architecture the number of bits for the discrete levels 'l' is 5,4 and 3 for Gaussian, Trapezoidal, and Triangular respectively, that is, the grade has been discretized into 32, 16 and 8 levels respectively.

V. FPGA RESOURCE UTILIZATION

The proposed structure of MAX-MIN calculator has been implemented in SPARTAN-3 XC3S50 XILLINX FPGA. This FPGA consists of 768 slices, 1536 4-input LUTs and 124 bonded input/output buffers (IOB). Table-1 gives the comparative analysis for implementation of triangular, trapezoid and gaussian MAX-MIN calculator circuits.This combined structure of triangular , trapezoid and gaussian consumes very less number of FPGA resources. The main feature of combined structure adaptively works for triangular, gaussian and trapezoidal membership functions together. There is a further scope for improvement in the proposed design by using pipelining and use of new methodology to further reduce the area and latency. The resource utilization clearly shows that the proposed architecture is area, power and speed efficient in comparison to the existing architectures of MAX-MIN calculator.

VI. CONCLUSION

In this paper, the problem of matching degree calculation between the fuzzified input and antecedent MF's has been addressed by proposing and implementing a MAX-MIN calculator circuit to improve the fuzzy inferencing. The designed MAX-MIN calculator calculates the MD between not only one type of MF's but between three types of MF's. In spite of processing more points and is handling MMF's the proposed architecture is area and power efficient and more flexible.

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