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Development of Customized Interrupt Controller Logic

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Abstract: Development of Customized Interrupt Controller logic is described in this paper. It explains the concepts and development of Interrupt Controller logic for applications where the available Programmable Interrupt Controllers cannot be used. The logic is developed using Verilog HDL. As the total logic is realized with hardware programmable devices like FPGAs, there is a significant improvement in space, power consumption, cost, speed and reliability. The logic can be integrated with any other logic on same or different chips to make the whole system a very user friendly in an economical and reliable manner.

Keywords: FPGA, Interrupt, Controller, Microprocessor, Programmable, Digital.

I. INTRODUCTION

A. Introduction to Programmable Interrupt Controller

Every system is designed to perform certain tasks. In case of an embedded system, all the tasks are pre-defined and pre-programmed. Embedded system makes use of a micro-processor/microcontroller to control and coordinate with different types of input and output devices called peripheral devices. A single microcontroller can serve several devices. There are two ways to do that. They are interrupts and polling. In Polling method, the microcontroller continuously monitors the status of a given device. When the condition is met, it performs the service. After that it moves on to monitor the next device until every device is serviced. Although polling can monitor the status of several devices and serve each of them as certain conditions are met, it is not efficient as far as the use of microcontroller is concerned. In interrupt method, whenever any device needs its service, the device notifies the microcontroller by sending it an interrupt signal. Upon receiving an interrupt signal, the microcontroller interrupts whatever it is doing and serves the device. The program which is associated with the interrupt is called Interrupt Service Routine (ISR) or Interrupt Handler. The advantage of interrupts is that microcontroller can serve many devices, not all the devices at the same time. Each device can get the attention of the microcontroller based on the priority assigned to it. In the interrupt method, micro-controller can ignore(mask) a device request for service.

This is not possible in case of polling method. Moreover, microcontroller's time is not wasted in interrupt method. The lntel 8259A Programmable lnterrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements. The Programmable Interrupt Controller functions as an overall manager in an interrupt driven system environment. It receives the interrupt requests from various devices or equipments, prioritizes the input interrupt requests based on the configured data, checks if the input is of top priority than the level currently being serviced, and generates an interrupt to the CPU. Block Diagram of Programmable Interrupt Controller is shown in Fig.1.

B. Limitations of Programmable Interrupt Controllers

- One PIC IC accepts only eight interrupt requests. If more inputs are there, additional ICs have to be cascaded.
- Maximum of eight ICs can be cascaded. Hence only 64 inputs can be handled with this mechanism. If the input interrupt requests are more than 64, the mechanism of interrupt handling by PIC ICs is not feasible.
- Initialization has to be done based on the system application.
- As the number of ICs increase Space, Cost, Power Consumption increases.

C. Current Design Challenges

Present day designers have to keep the following five points before carrying out any new design. They are:

- Design should be compact. That is logic should occupy less space. This is possible only when less number of components is used for the logic[1].
- Design cost should be justifiable. There should not be additional cost for unwanted or unused resources in the logic designed. This is possible by using the programmable devices for realizing the customized logic[2],[3].
- Logic should consume less power. This is possible by using thin silicon devices and shutting down the logic not being used at any time[4].

- Design up gradation / modification should be possible to meet the varying demands of customer at any time. This is possible only when suitable programmable devices are selected and the apt connectivity is provided in the logic[5].
- Design time should be less and problems encountered at any stage should be rectified without any change in the hardware. Because any change in the hardware involves much of the time, money and manpower. This will be feasible with hardware programmable devices like CPLDs and FPGAs[6].
- Designing with CPLDs / FPGAs will reduce the design time, increase design flexibility, makes design compact and reasonably economical, reduces power consumption and improves reliability[1],[7],[8].

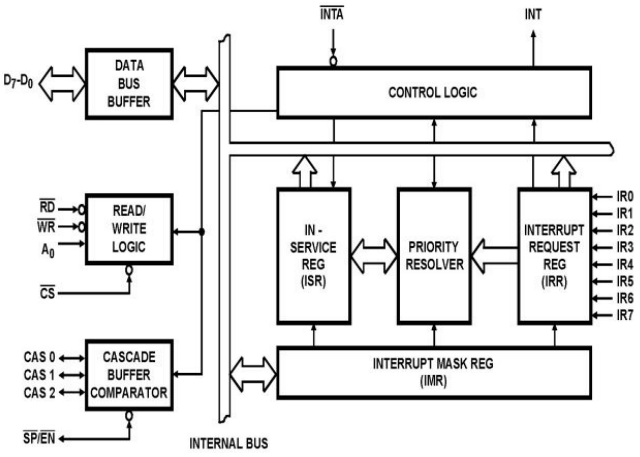

Fig.1.Block Diagram of Programmable Interrupt Controller.

II. IMPLEMENTATION OF CUSTOMIZED INTERRUPT CONTROLLER

A. Customized Interrupt Controller

Interrupt Controller developed for the customized application of Versatile Multiplexer Logic is described here. Interface diagram is shown in Fig.2. There are two interrupt controller circuits implemented in FPGA. One is for interrupts coming from service cards. Other interrupt is for interrupts coming from On-board peripherals.

1. Interrupt Controller Circuit For On-Board Peripherals: Interrupt inputs to this logic are interrupts from I2C Controller2,I2C Controller1, LIU, and 32 HDLC Controllers. One single interrupt HDLC_INT is generated when any of the 32 interrupts are activated. These interrupts are stored in HISR1 and HISR2 registers. Individual interrupts can be enabled or disabled by writing the HIER1 and HIER2 registers. Similarly, writing in HIMR1 and HIMR2 registers can mask them. All these interrupt inputs are active high. When any one of the interrupts I2C1_INT, I2C2_INT, HDLC_INT and LIU_INT is activated, REG_INT will be enabled (active low). These interrupts are stored in the Interrupt Status Register (REG_ISR). All interrupts are indicated as active high in ISR. Individual interrupts can be enabled or disabled by writing the REG_IER register. Similarly, writing in REG_IMR register can mask them. Once REG_INT is asserted, DSP reads the REG_ISR to know the interrupt source. In case of HDLC_INT, DSP has to read the HISR1 and HISR2 registers to know which HDLC controller has generated interrupt. After reading the REG_ISR, DSP enters the corresponding interrupt service routine. In the service routine DSP should first clear the corresponding interrupt enable bit. Then automatically that particular interrupt status bit in REG_ISR will be cleared. At the end of the service routine, DSP should again enable that bit in REG_IER. This mechanism helps DSP to service all the routines continuously and in a sequential manner.

2. Interrupt Controller circuit for Service Cards: Interrupt inputs to this logic are interrupts from service cards. All these interrupt inputs are active high. When any one of these interrupts is activated, SC_INT will be enabled (active low). These interrupts are stored in the Interrupt Status Register (SC_ISR). All interrupts are indicated as active high in SC_ISR. Once SC_INT is asserted, DSP reads the SC_ISR to know the interrupt source. After reading the SC_ISR, DSP enters the corresponding interrupt service routine. In the service routine DSP should first clear the corresponding interrupt enable bit. Then automatically that particular interrupt status bit in SC_ISR will be cleared. At the end of the service routine, DSP should again enable that bit in SC_IER. This mechanism helps DSP to service all the routines continuously and in a sequential manner[9].

B. Advantages of Customized Interrupt Controller

- The logic for CIC requires less circuitry.
- It requires no initialization.
- It is designed for the customized application for avoiding unnecessary logic on FPGA.
- It is designed to be a part of the main system built on FPGA.
- It ensures high flexibility.

C. Resource Utilization and Observation

Details of Resource Utilization and Design Summary are shown in Table-1.

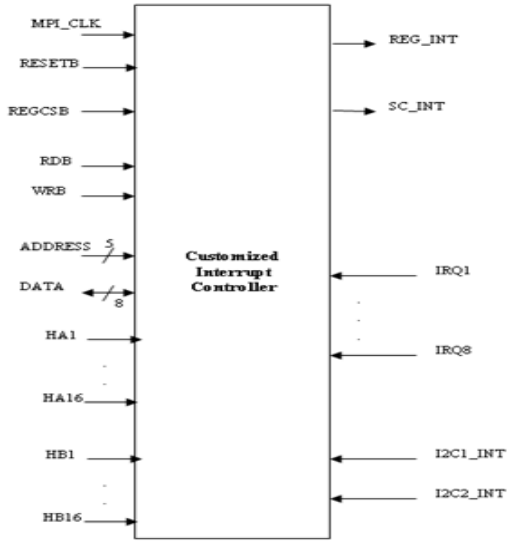

Fig.2. Customized interrupt controller logic.

TABLE I: Design Summary and Resource Utilization

int_control Project Status (10/30/2015 - 22:53:25)			
Project File:	Interrupt_Controller.xise	**Parser Errors:**	No Errors
Module Name:	int_control	**Implementation State:**	Programming File Generated
Target Device:	xc6slx45-3fgg484	• **Errors:**	No Errors
Product Version:	ISE 14.5	• **Warnings:**	12 Warnings (12 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	180	54,576	1%	
Number used as Flip Flops	180			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	201	27,288	1%	
Number used as logic	200	27,288	1%	
Number using O6 output only	158			
Number using O5 output only	0			
Number using O5 and O6	42			
Number used as ROM	0			
Number used as Memory	0	6,408	0%	
Number used exclusively as route-thrus	1			
Number with same-slice register load	1			
Number with same-slice carry load	0			
Number with other load	0			
Number of occupied Slices	80	6,822	1%	
Number of MUXCYs used	0	13,644	0%	
Number of LUT Flip Flop pairs used	209			
Number with an unused Flip Flop	62	209	29%	
Number with an unused LUT	8	209	3%	
Number of fully used LUT-FF pairs	139	209	66%	
Number of unique control sets	8			
Number of slice register sites lost to control set restrictions	12	54,576	1%	
Number of bonded IOBs	62	316	19%	
IOB Flip Flops	1			
Number of RAMB16BWERs	0	116	0%	
Number of RAMB8BWERs	0	232	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	8	0%	
Number of ILOGIC2/ISERDES2s	0	376	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	376	0%	
Number of OLOGIC2/OSERDES2s	1	376	1%	
Number used as OLOGIC2s	1			
Number used as OSERDES2s	0			
Number of BSCANs	0	4	0%	
Number of BUFHs	0	256	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	58	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	4	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	3.38			

Performance Summary [-]			
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Fri Oct 30 22:52:05 2015	0	12 Warnings (12 new)	1 Info (1 new)
Translation Report	Current	Fri Oct 30 22:52:17 2015	0	0	0
Map Report	Current	Fri Oct 30 22:52:39 2015	0	0	6 Infos (6 new)
Place and Route Report	Current	Fri Oct 30 22:52:56 2015	0	0	3 Infos (3 new)
Power Report					
Post-PAR Static Timing Report	Current	Fri Oct 30 22:53:05 2015	0	0	4 Infos (4 new)
Bitgen Report	Current	Fri Oct 30 22:53:22 2015	0	0	0
Secondary Reports [-]					
Report Name	**Status**	**Generated**			
WebTalk Report	Current	Fri Oct 30 22:53:23 2015			
WebTalk Log File	Current	Fri Oct 30 22:53:25 2015			

III. CONCLUSION

Customized Interrupt Controller logic is a part of Versatile Multiplexer logic. VMUX is a part of telecom system and plays a crucial role for effective functioning of the access network and makes the subscriber effectively interacted with the switching network. The advantage of CIC logic is it can be integrated with rest of the system in a single chip to reduce the number of components for saving the space, time, money, power and increasing reliability. Moreover it makes the design hierarchy flexible. Any suitable hardware programmable device like FPGAs of different family make having the required logic elements can be used for this purpose without any modification to the design architecture.

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