Development of Customized Interrupt Controller Logic

T. HARNATH¹, K. LAL KISHORE²

1Electronics Corporation of India Limited, Hyderabad, India, E-mail: harnath.t@gmail.com.
2Jawaharlal Nehru Technological University, Ananthapur, AP, India, E-mail: lalkishorek@yahoo.com.

Abstract: Development of Customized Interrupt Controller logic is described in this paper. It explains the concepts and development of Interrupt Controller logic for applications where the available Programmable Interrupt Controllers cannot be used. The logic is developed using Verilog HDL. As the total logic is realized with hardware programmable devices like FPGAs, there is a significant improvement in space, power consumption, cost, speed and reliability. The logic can be integrated with any other logic on same or different chips to make the whole system a very user friendly in an economical and reliable manner.

Keywords: FPGA, Interrupt, Controller, Microprocessor, Programmable, Digital.

I. INTRODUCTION

A. Introduction to Programmable Interrupt Controller

Every system is designed to perform certain tasks. In case of an embedded system, all the tasks are pre-defined and pre-programmed. Embedded system makes use of a microprocessor/microcontroller to control and coordinate with different types of input and output devices called peripheral devices. A single microcontroller can serve several devices. There are two ways to do that. They are interrupts and polling. In Polling method, the microcontroller continuously monitors the status of a given device. When the condition is met, it performs the service. After that it moves on to monitor the next device until every device is serviced. Although polling can monitor the status of several devices and serve each of them as certain conditions are met, it is not efficient as far as the use of microcontroller is concerned. In interrupt method, whenever any device needs its service, the device notifies the microcontroller by sending it an interrupt signal. Upon receiving an interrupt signal, the microcontroller continuously monitors the status of a given device. The program which is associated with the interrupt is called Interrupt Service Routine (ISR) or Interrupt Handler. The advantage of interrupts is that microcontroller can serve many devices, not all the devices at the same time. Each device can get the attention of the microcontroller based on the priority assigned to it. In the interrupt method, microcontroller can ignore(mask) a device request for service.

This is not possible in case of polling method. Moreover, microcontroller’s time is not wasted in interrupt method. The Intel 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements. The Programmable Interrupt Controller functions as an overall manager in an interrupt driven system environment. It receives the interrupt requests from various devices or equipments, prioritizes the input interrupt requests based on the configured data, checks if the input is of top priority than the level currently being serviced, and generates an interrupt to the CPU. Block Diagram of Programmable Interrupt Controller is shown in Fig.1.

B. Limitations of Programmable Interrupt Controllers

- One PIC IC accepts only eight interrupt requests. If more inputs are there, additional ICs have to be cascaded.
- Maximum of eight ICs can be cascaded. Hence only 64 inputs can be handled with this mechanism. If the input interrupt requests are more than 64, the mechanism of interrupt handling by PIC ICs is not feasible.
- Initialization has to be done based on the system application.
- As the number of ICs increase Space, Cost, Power Consumption increases.

C. Current Design Challenges

Present day designers have to keep the following five points before carrying out any new design. They are:

- Design should be compact. That is logic should occupy less space. This is possible only when less number of components is used for the logic[1].
- Design cost should be justifiable. There should not be additional cost for unwanted or unused resources in the logic designed. This is possible by using the programmable devices for realizing the customized logic[2],[3].
- Logic should consume less power. This is possible by using thin silicon devices and shutting down the logic not being used at any time[4].
Design upgradation / modification should be possible to meet the varying demands of customer at any time. This is possible only when suitable programmable devices are selected and the apt connectivity is provided in the logic[5].

Design time should be less and problems encountered at any stage should be rectified without any change in the hardware. Because any change in the hardware involves much of the time, money and manpower. This will be feasible with hardware programmable devices like CPLDs and FPGAs[6].

Designing with CPLDs / FPGAs will reduce the design time, increase design flexibility, makes design compact and reasonably economical, reduces power consumption and improves reliability[1],[7],[8].

Once REG_INT is asserted, DSP reads the REG_ISR to know the interrupt source. In case of HDLC_INT, DSP has to read the HISR1 and HISR2 registers to know which HDLC controller has generated interrupt. After reading the REG_ISR, DSP enters the corresponding interrupt service routine. In the service routine DSP should first clear the corresponding interrupt enable bit. Then automatically that particular interrupt status bit in REG_ISR will be cleared. At the end of the service routine, DSP should again enable that bit in REG_IER. This mechanism helps DSP to service all the routines continuously and in a sequential manner.

2. Interrupt Controller circuit for Service Cards: Interrupt inputs to this logic are interrupts from service cards. All these interrupt inputs are active high. When any one of these interrupts is activated, SC_INT will be enabled (active low). These interrupts are stored in the Interrupt Status Register (SC_ISR). All interrupts are indicated as active high in SC_ISR. Once SC_INT is asserted, DSP reads the SC_ISR to know the interrupt source. After reading the SC_ISR, DSP enters the corresponding interrupt service routine. In the service routine DSP should first clear the corresponding interrupt enable bit. Then automatically that particular interrupt status bit in SC_ISR will be cleared. At the end of the service routine, DSP should again enable that bit in SC_IER. This mechanism helps DSP to service all the routines continuously and in a sequential manner[9].

B. Advantages of Customized Interrupt Controller

- The logic for CIC requires less circuitry.
- It requires no initialization.
- It is designed for the customized application for avoiding unnecessary logic on FPGA.
- It is designed to be a part of the main system built on FPGA.
- It ensures high flexibility.

C. Resource Utilization and Observation

Details of Resource Utilization and Design Summary are shown in Table-1.

![Fig.1. Block Diagram of Programmable Interrupt Controller.](image1)

**Fig.1.** Block Diagram of Programmable Interrupt Controller.

**II. IMPLEMENTATION OF CUSTOMIZED INTERRUPT CONTROLLER**

**A. Customized Interrupt Controller**

Interrupt Controller developed for the customized application of Versatile Multiplexer Logic is described here. Interface diagram is shown in Fig.2. There are two interrupt controller circuits implemented in FPGA. One is for interrupts coming from service cards. Other interrupt is for interrupts coming from On-board peripherals.

1. Interrupt Controller Circuit For On-Board Peripherals:

Interrupt inputs to this logic are interrupts from I2C Controller, I2C Controller1, LIU, and 32 HDLC Controllers. One single interrupt HDLC_INT is generated when any of the 32 interrupts are activated. These interrupts are stored in HISR1 and HISR2 registers. Individual interrupts can be enabled or disabled by writing the HIER1 and HIER2 registers. Similarly, writing in HIMR1 and HIMR2 registers can mask them. All these interrupt inputs are active high. When any one of the interrupts I2C1_INT, I2C2_INT, HDLC_INT and LIU_INT is activated, REG_ILT will be enabled (active low). These interrupts are stored in the Interrupt Status Register (REG_ISR). All interrupts are indicated as active high in ISR. Individual interrupts can be enabled or disabled by writing the REG_IER register. Similarly, writing in REG_IMR register can mask them.

![Fig.2. Customized interrupt controller logic.](image2)

**Fig.2.** Customized interrupt controller logic.
III. CONCLUSION

Customized Interrupt Controller logic is a part of Versatile Multiplexer logic. VMUX is a part of telecom system and plays a crucial role for effective functioning of the access network and makes the subscriber effectively interacted with the switching network. The advantage of CIC logic is it can be integrated with rest of the system in a single chip to reduce the number of components for saving the space, time, money, power and increasing reliability. Moreover it makes the design hierarchy flexible. Any suitable hardware programmable device like FPGAs of different family make having the required logic elements can be used for this purpose without any modification to the design architecture.

IV. REFERENCES


Author's Profile:

T.Harnath received B.E degree in Electronics & Communications Engineering from Osmania University, Hyderabad, India in 1995 and M.S in ECE from Jawaharlal Nehru Technological University, Hyderabad, India in 2008. He has also received MBA in Operations Research from Indira Gandhi National Open University, Delhi in 2008. He has worked in Advanced Radio Masts Ltd, Hyderabad and Avantel Communications Ltd, Hyderabad. He is working in Electronics Corporation of India Limited, Hyderabad since 1998, presently he is Technical Manager. He has around 20 years of experience in Research and Development of various telecom equipments and communication systems. He is pursuing Ph D in ECE under the guidance of Prof K. Lal Kishore from JNTU, Hyderabad. His areas of interest include Embedded Systems, VLSI Design, Communication Systems and Networking. He is a member of International Institute for Electrical and Electronics Engineers (IEEE), Institute of Engineers India (IEI) and Institute of Electronics and Telecommunications Engineers (IETE).

Prof. K. Lal Kishore, held the position of Vice Chancellor of Jawaharlal Nehru Technological University Ananthapur (JNTUA). He had also held the positions of Rector and Registrar of JNTU Hyderabad. As Professor of ECE, he has more than 34 years of experience in teaching and 25 years in research. He obtained B.E from OU, M.Tech and Ph.D from IISc., Bangalore. His research interests include Electronics Devices, VLSI, Micro Electronics & Instrumentation. He produced 11 Ph.Ds and submitted 3 Ph.D theses for evaluation. He has been honored with State Award as the Best Teacher, from Government, AP, for the year 2004, Sir Mokshagundam Visvesvaraya Award from Government of Andhra Pradesh and Institute of Engineers in 2010, Prof. SVC Aiya Memorial Award from 11th IETE in 2007, Distinguished Indian Award from ICSCI in 2007, First Bapur Seetharam Memorial Award from IETE in 1986 and Certificate of Recognition from DEC, Debrezeit. He is Fellow of Institute of Engineers and Institute of Electronics & Telecommunication Engineers. He is Member of IEEE, ISTE, ISHM and Chairman of IETE Centre, Hyderabad News in 2011. He has 152 Research publications in reputed International/National Journals and Conferences. He has authored 06 books and implemented 07 sponsored research projects. He has been a member of Several Governmental Committees. He has been the Convener of ECET during the years 2000, 2001 & 2005. He has served as Registrar, Rector, Director of R&D Cell, SIT, UGC-Academic Staff College, Academic and Planning, School of Continuing and Distance Education of JNTUH and as Principal of JNTU College of Engineering, Hyderabad. He delivered number of expert lectures and key note addresses on various technical topics. He has organized numerous workshops and participated in several TV panel discussions. He has visited Research Centers/Universities at France, UK, Israel, Hong Kong, Ireland, and Ethiopia.