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Design of Real-Time Traffic Control System using Verilog

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Abstract: In this project we projected a design of traffic light control system (TLC) to manage the road traffic and clear the way for the ambulance. The steps that are followed in this project are proposing the idea, writing code, simulate, synthesis and finally the system has been successfully verified. The controller is designed by using Verilog Hardware Descriptive Language, Simulated and Synthesized using XILINX ISE tool.

Keywords: FSM, Simulation, Traffic Light Control System (TLC), Verilog, Xilinx ISE Simulator.

I. INTRODUCTION

Now a days Traffic jamming is a serious predicament in many of the cities and towns throughout the globe. To travel within the cities to the place of work or restoration has become an issue to the commutates all along. Because of this public lose time, money and mostly energy resources will be drained due to frequent use of automobiles. In the past many ideas have come up to reduce the complexity of the traffic congestion. Generally the time allotment is unchanging for east and west side, in the same way for north and south side in a traffic light controller near cross roads. To crack these traffic related issues we are emerging a system which reduces the traffic jam The traffic light arrangement works on the particular switching of Red, Green and Yellow lights in a sequence and whenever an ambulance is in the traffic it is detected using a sensor and the light automatically switches to green and all other roads are blocked

II. OPERATION OF TRAFFIC CONTROL SYSTEM

In this paper we are going to design a time based traffic light control system for a junction of having four ways. We are internally designing a decrement counter which is used to display the signal time in a decrement order and also to change the signal from on path to another sequentially. In the conventional traffic light controller we were not able to change the signals during emergencies like when an ambulance enters in any path and also we there was not able to change the signal time during peak and non-peak hours. So we are overcoming these problems in this paper. In addition to the time based traffic controlling, we are placing siren sensors in all four paths. When an ambulance enters in a particular path, the siren sensor senses the arrival of the ambulance in that path. The present signals and the present time will be paused; traffic signal for that particular path will be made green so that the ambulance passes smoothly. As soon as the ambulance leaves, the previous signals and also the time will be resumed. In this paper we have an input signal called peak. During non-peak hours this signal will be low and the signal time will be for sixty seconds. In peak hours there will be more vehicles. So the signal time should also be increased. During peak hours the peak signal will be made high. When the peak signal made high, the signal will stay for one hundred and twenty seconds for the smooth movement of the vehicles.

III. DESIGN METHODOLOGY

A Traffic Light Controller can be deliberated with certain conventions. Primarily Red signal is ON in North, East, West and South direction. Whenever the reset pin is made high there will be a way for the traffic which is in the north and all other paths are blocked and the sequence follows. Whenever an ambulance is in the traffic it is detected using a sensor and the light automatically switches to green and all other roads are blocked.

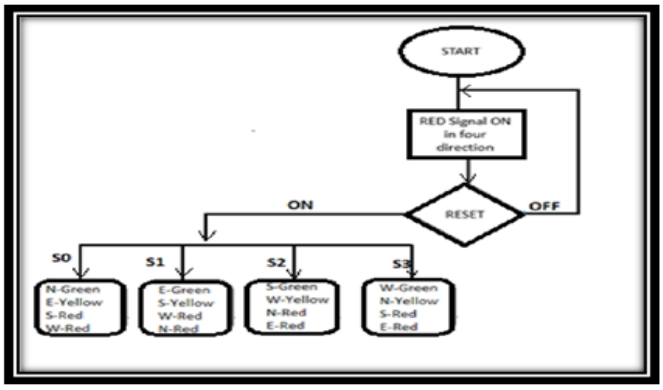

Fig.1.

The design is synchronous with the clock clk. rst is a one bit signal used to reset the system and it is synchronous to the clock signal. amb_a, amb_b, amb_c and amb_d are the siren

sensor output from path a, path b, path c and path d respectively. Peak is a one bit input signal used to indicate whether it is a peak hour or a non-peak hour. Time_out is an output signal used to represent the signal timing for every path. The other output signals represents the path_siglal for example a_green reptesents green signal in path a. Synthesis is a process of getting gate level netlist from RTL model of a circuit defined in Hardware Description Language. It a process in which a design behavior that is modeled using a HDL i.e behavioural level is translated into an implementation containing of logic gates i.e. structure. Synthesis can be done by synthesis tools whose output is a netlist. After synthesizing the code, we can able to view the RTL Schematic of our design. This RTL schematic is generated after the synthesis process. It shows a representation of the pre-optimized design in terms of generic symbols, such as adders, multipliers, counters, NOT gates, AND gates, and OR gates, that are independent of the targeted Xilinx device. The Traffic light controller System is designed by using Verilog HDL and simulated using Xilinx ISE tool. The figs.2 and 3 shown below are the RTL Schematics obtained of the proposed design.

Fig.2. The block diagram of Real-Time Traffic Light controller system after synthesis.

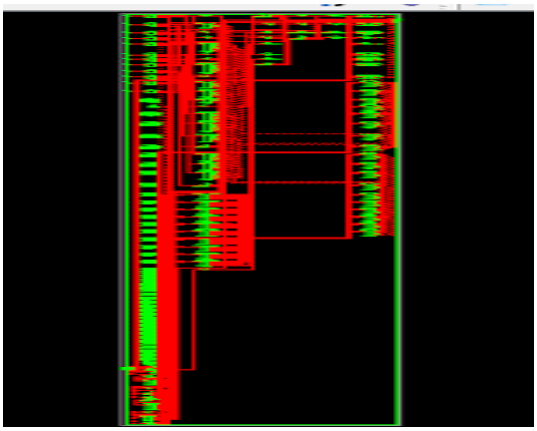

Fig.3. The RTL schematic of Real_Time Traffic Light Control System which displays gates and elements used in digital circuitry.

IV. SIMULATION RESULTS

Simulation a process of verifying the functionality of the digital design. to verify we require testbench as shown in Fig.4. testbench is a program in which the inputs are declared as reg and outputs are declared as wire and in this some ideal values are given in order to verify the behavior of the design as it is working as the required deisgn or not.

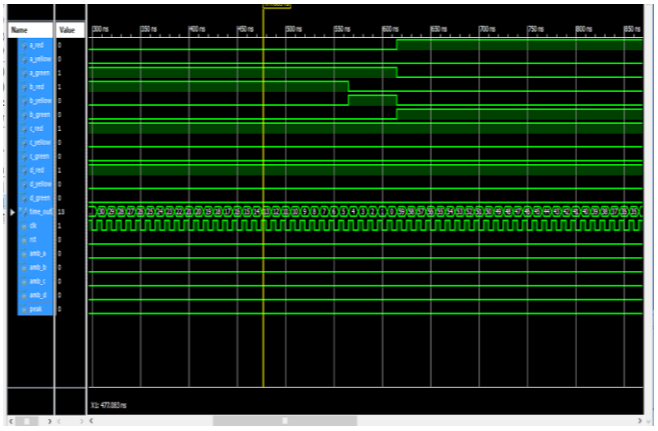

Fig.4. The simulation wave form shows the operation of Traffic Controll Systems.

Initially the rst is high so all the paths have red signal and whenever the rst is made low and there were no ambulances in the paths so only path a has green signal and all other paths are blocked and whenever the reset is high and peak is high the ambulance in path will have green signal and works sequentially.

V. CONCLUSION

In this paper we have designed an efficient, reliable and intelligent traffic light controller using Verilog Hardware Descriptive Language. This helps in solving the traffic related issues. As it differentiates peak hours and non-peak hours it saves time. Also as it clears the way for ambulance it saves life. The future scope of this project is it can be directly applied in real time by employing density based automatic traffic control.

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