Design & Implementation of VGA Display System Based on CPLD and Dual Memory

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Abstract: The paper designs a VGA image and writing display controller with FPGA chip based on EDA technology. The system designs VGA display that produces the image signal and the control signal with FPGA. In the process of designing the system deposited the color image and transfer, finally completes video data processing through the simulation and downloading only based on the single chip. Due to the lack of professional VGA display controller in Most embedded systems, splash screen; even blank screen problems may appear while displaying the high-resolution video image. The design illustrates the implement method of VGA display controller, which combines CPLD and SRAM. First, the design stores data that gets from the processor in the SRAM and then reads them out in form of VGA display interface standard into D/A converter which will convert the data into analog signals to display. The whole operation above is controlled by CPLD. So such a design can effectively solve the problems caused by insufficient bandwidth in the displaying, what's more, it can reduce the pressure of the CPU and here the extension of the project here we go for implementing of dual memory which is used to store the dual images and retrieves the images information with high resolution pixels which display on VGA. The article not only gives the internal detailed design of CPLD, which includes generation of VGA timing signal, finite state machine and logic control, but also presents analysis of practical tests rendering. The system has been successfully used in the digital language teaching Products.

Keywords: CPLD, VGA, Memory, Verilog.

I. INTRODUCTION

Generally to display the output on the monitor the logic analyzer uses C.P.U. But if we use such logic analyzer then there is problem of extra software that means it requires extra software for proper function. So by eliminating the use of CPU and to display the data on the monitor VGA display based on the CPLD and SRAM is necessary. With the help of such design data that gets from the controller in the SRAM is stores and then convert the data into analog signals to display on the VGA monitor. And all this operation is controlled by CPLD. Before going to see system development of this design, we have to see its major component like, what CPLD is and which program downloading technique is used. CPLD (complex programmable logic device) is a device erasable programmable logic device that can be programmed with schematic and behavioral design CPLDs, which provides the features in between FPGA and PLAs. CPLD consist of number of circuits which contain series of gates and macro cells, each macro cell capable of implementing combinational and registered function. CPLD are ideal for complex box with large number of input. It require less board pace than FPGA, hence it has less board complexity than FPGA. In this design CPLD operates using its sampler module. This module is responsible to sampling appearance of the CPLD controller. CPLD also operate using Displayer module, this module takes care of the visuals of the oscilloscope. With the development of embedded system and its popularization in each industry, the requirements of the market for display also become higher and higher, and terminal video image display has become an important part of the development of the system.

In fact, VGA interface displayer is an important terminal display device of computer and various intelligent instrument equipment’s. Due to the unified standard and relatively mature technology of VGA interface, it has always been used as the connected interface between the computer and external displayer. Now most of the embedded processor only integrated the LCD controller without VGA controller [1], therefore, we need to covert LCD signal to VGA interface signal. For now, the most widely used program chooses an appropriative conversion chip to handle. The advantage of this scheme is that it’s easy to use, but at the same time, there also exists defect. First, when we want to show a 16-bit true color image, which has resolution of 1024*768 and 60 Hz field frequency, general processor may appear screen dithering, and even temporary blank screen when displaying the picture in above mode. This attributed to the internal of general processor do not
have graphic processing module, and it cannot load such huge image data’s transmission. Another point is that it’s not easy to upgrade and update, once we want to show different resolution pictures, it needs to design the hardware circuit again and again, and sometimes even needs to replace conversion chip, then development cycle will get longer, and in a certain extent, cost will increase, which is not conducive to upgrade of the product. In view of the above question, this design put forward a method which combined CPLD with SRAM to realize the control of VGA display. In other words, pulsing this module between the processor and display so that it could store the data, which transfer from the processor, to high speed of SRAM memory, and each frame data that VGA interface displayer received are read from SRAM according to the standard, consequently, it can completely satisfy the requirement of VGA video display standard. This system is suitable for terminal display of all kinds of embedded systems. The advantages of the design are simple circuit structure, flexible design, high stability and transplantation convenience etc.

II. LITERATURE REVIEW

This chapter is a description of the literature that was read in order to solve the oscilloscope problem. No literature has been found on this specific problem. There is however plenty of literature on the individual parts used to solve this problem. These parts are the Oscilloscope, the VGA monitor and the FPLD. I felt that it would be a good idea to read as much as necessary about these different parts.

III. SYSTEM STRUCTURE

The design is a VGA display system based on the CPLD and SRAM, and it will be applied to a variety of embedded display terminals, especially digital language teaching system terminal interface display. The hardware circuit diagram of the system is shown in Figure 1. It is mainly composed of VGA controller, D/A converter and SRAM. To display images or videos, it should have a data source, and the data of system come from the application programs of computer. So it needs to program the corresponding application program, and then transmit data to the system through the USB interface. Intermediate using special USB conversion chip CH341 to convert the data format to parallel format data, and so that CPLD collect data conveniently according to the agreement. VGA display image data volume is usually huge, and the built-in ROM of CPLD is difficult to meet such a large amount of data, so there needs external RAM to store the data. Input signal of the VGA display is an analog signal (line and field signal is digital signal), so before getting into the VGA interface the data collected from parallel port must be transferred by the D/A converter. This design uses the Altera Company’s MAX series II chip as the core hardware circuit to design. The computer sends the picture data, whose field frequency is less than 30Hz and resolution is the 800*600, is based on the 16-bit RGB model. So, through this we can verify the feasibility of the system program.

A. Design of VGA controller

The VGA controller handles the low-level details of communicating with a monitor over a VGA connector. The VGA controller is implemented in VGA.v. It controls the DE2-115’s video digital-to-analog converter, the Analog Devices ADV7123. The VGA controller maintains a 2-dimensional array of 15-bit values in video memory. The width of the array is 640 (0-639), and the height of the array is 480 (0-479). Each value represents the color of a pixel: bits 14-10 specify the amount of red; bits 9-5 specify the amount of green; and bits 4-0 specify the amount of blue (this is known as 15 bit RGB). Pixel coordinates are denoted as (x, y). The coordinate of the upper left pixel is (0, 0); the coordinate of the lower right pixel is (639,479). VGA_command and VGA_response implement the standard I/O protocol. The command parameters are VGA_write, vga_x1, vga_y1, vga_x2, vga_y2, and VGA_color_write. If the E100 program sends a command with VGA_write=1, this signifies that the program wants to set the color of a rectangle to VGA_color_write.

The upper-left corner of the rectangle is (vga_x1, vga_y1), and the lower-right corner of the rectangle is (vga_x2, vga_y2). VGA_x1 must be less than or equal to vga_x2, and vga_y1 must be less than or equal to vga_y2. If the E100 program sends a command with VGA_write=0, this signifies that the program wants to read the color of the pixel at (vga_x1, vga_y1). In this case, the color of this pixel will be returned in the response parameter VGA_color_read. Ase100 simulates the VGA controller accurately enough for you to test your device driver and to run assembly-language programs. Click the Save VGA button to save the contents of VGA memory to a file. Many of your projects will display pictures on the VGA monitor. See this handout for help in creating these pictures in the E100 color format.

B. VGA sequence

VGA (Video Graphics Array) is a video transmission standard, which launched with PS/2 by the IBM in 1987, and it has the advantages of high resolution, fast display speed and rich color, so it is widely used in area of color display [2]. VGA display also needs a standard timing signal, only in this way image data can be displayed accurately on the monitor. VGA interface signal mainly have five signals, they are line synchronous signal HS, field
synchronous signal VS and three primary color signals of RGB [3], and line and field synchronizing signals is the main control signal. This design uses the programmable logic device CPLD to produce corresponding pulse signal according to the VGA timing standard. In the very log programmer, we can use the counter and trigger combination way to generate different resolution line, field synchronous clock signal. VGA interface sequence is shown in Figure.2. The above is the row (HSYNC) scan sequence diagram, it consists of sync pulse(ha), Back porch (hb), Display interval(he) and Front porch(hd) four parts. The sync pulse (ha) is to tell the display driver that this line will begin to show, while display interval(he) is line effective display section. In the chart, the line blanking refers to not effective display space, and this range of display data is invalid. The structure of following field sequential is similar to the row, but the only different between the two is the length of time. From the above analysis, the image available display area is combined line with field effective areas, so when writing the programs we can use line and field counters to determine the marker bit of effective area of image display. In this way, you can program line, field counters to determine the image display effective area, so as to produce the read address.

C. VGA Interface Timing Diagram

Fig2. VGA Interface Timing Diagram.

D. VGA Signal Generation

A VGA video signal contains 5 active signals:

- horizontal sync: digital signal, used for synchronization of the video
- vertical sync: digital signal, used for synchronization of the video
- red (R): analog signal (0-0.7 v), used to control the color
- green (G): analog signal (0-0.7 v), used to control the color
- blue (B): analog signal (0-0.7 v), used to control the color

By changing the analog levels of the three RGB signal all other colors are produced the electron beam must be scanned over the viewing screen in a sequence of horizontal lines to generate an image. The RGB color information in the video signal is used to control the strength of the electron beam

- The screen refresh process begins in the top left corner and paints 1 pixel at a time from left to right. At the end of the first row, the row increments and the column address is reset to the first column. Once the entire screen has been painted, the refresh process begins again.
- The video signal must redraw the entire screen 60 times per second to provide for motion in the image and to reduce flicker: this period is called the refresh rate. Refresh rates higher than 60 Hz are used in PC monitors.
- In 640 by 480-pixel mode, with a 60 Hz refresh rate, this is approximately 40 ns per pixel. A 25 MHz clock has a period of 40 ns.
- The vertical sync signal tells the monitor to start displaying a new image or frame, and the monitor starts in the upper left corner with pixel (0,0).
- The horizontal sync signal tells the monitor to refresh another row of 640 pixels.
- After 480 rows of pixels are refreshed with 480 horizontal sync signals, a vertical sync signal resets the monitor to the upper left corner and the process continues.
- During the time when pixel data is not being displayed and the beam is returning to the left column to start another horizontal scan, the RGB signals should all be set to black color (all zero).
- In a PC graphics card, a dedicated memory location is used to store the color value of every pixel in the display. This memory is read out as the beam scans across the screen to produce the RGB signals. This design uses a 16-bit true color image of 800*600 resolution and 60Hz field frequency to transfer. First of all, determining the frequency of the master clock according to the refresh rate, then using the clock frequency and resolution of the image to calculate the various parameters of line and field sequential. By checking the standard, you can find pixel master clock is 40 MHz, and the system clock of this design is 80 MHz, so that binary frequency can get the pixel clock which is needed. Then the system clock of the 80 MHz can output directly to SRAM chip which asks for higher speed of reading and writing.

The pixel clock period multiplied by the number of pixels can get the row total time, while the line total time multiplied by the number of line to get field total time, the other by parity of reasoning, thereby the table 1’s parameters can be come out. VGA monitor is displayed in a progressive scanning way which is scanned from left to right, from top to bottom. When scanning each row, there will have a period of blanking, and during this period, the display driver do not do any of the display, so do not send effective data to display in this meantime, otherwise the image display errors would be aroused, so as to the field blanking.
IV. RESULTS AND SIMULATION
Testing and Synthesis is carried out by Xilinx software is used in this article to synthesize, emulate and debug. Host computer sends the picture data down, then the system collects data through the appropriate programs and caches to the SRAM, finally, it reads the dual memory data for VGA display module. The VGA display standard resolution here we use is 800 * 600, and its refresh rate is 60Hz. Connecting VGA interface of System to the monitor, then issues the image data in the host computer (the computer), after that, we can see the

A. RTL Technology Schematic

![RTL Technology Schematic](image1)

Fig3.

B. Wave form

![Wave form](image2)

Fig6.

V. CONCLUSION
The experiments show that the picture is correctly displayed on the monitor, and it has good stability, good visual effects, and the naked eye can not feel that the image is refreshed. The innovation of the system is that it puts forward the CPLD or FPGA, Memory (SDRAM, FLASH and other memory devices) devices, as well as the combination of the module of digital-to-analog converter, then it takes external memory as a VGA video memory, finally, it achieves a stable display of VGA interface. Using this scheme can reduce the pressure of embedded system of CPU, what’s more, it effectively solve the original conversion system monitors problems of jitter, flash screen, and even blank screen problems. This system also applies to the microcontroller to control the display, while interface can also use the parallel port. The microcontroller can use ATmega128 to control, so that you can use the MCU to control VGA port to display. This design has certain practicability and value of popularization.

VI. REFERENCES
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