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Design of High Efficient Traffic Light Controller using Verilog HDL

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Abstract: Traffic lights are the signaling devices used to manage traffic on multi-way road. These are positioned to control the competing flow of the traffic at the road intersections to avoid collisions. By displaying lights (red, yellow and green), they alternate the way of multi-road users. The implementation of traffic Light Controller can be through a Microcontroller, Field Programmable Gate Array or Application Specific Integrated Circuit. FPGA is that it has numerous merits over microcontroller in TLC design. Some of these merits are high speed of operation, more number of input/output ports and better performance. In IA-TLC density of traffic is sensed by using IR sensors throughout day and night, and accordingly time is allotted for users to pass. Other advantages of this system are: i) System senses emergency vehicles on the individual road moreover it gives priority to the traffic of that particular road where the emergency vehicles is sensed. ii) Finds out defaulter who crosses the red signal by capturing images using camera. The system has been implemented in software using Xilinx 14.3.

Keywords: FPGA, Xilinx, Traffic Light Controller.

I. INTRODUCTION

Traffic jamming is a critical predicament in many of the cities and towns all over the world. Traffic congestion has been causing many setbacks and challenges in the major and most occupied cities all over the globe. To travel within the cities to the place of work or recreation has become a big problem to the commutates all along. Due to These problems people lose time, money and most importantly the energy resources will be exhausted due to the continual use in the automobiles. This traffic jam directly impacts the productivity of the workers, traders, suppliers and in all effecting the market and raising the prices of the commodities in a way. To solve these traffic related problems, we have to build new conveniences & infrastructure but at the same time make it smart. The only drawback of making new roads on facilities is that it makes the Surroundings more congested, but then this will make a way to have new ways to ease the traffic. Perhaps all the countries are working to accommodate the traffic flow and advance transportation and reduce the demand of vehicle use. We have to build new facilities and infrastructure making its use smarter for its efficient use. For this many ideas about the traffic light systems have come up in the recent past to simplify the complex problem of the traffic congestion. Mostly we see that the time allocation is fixed for east and west side, similarly for north and south direction in a traffic light controller at crossroads. Traffic light controller (TLC) has been implemented using microcontroller FPGA, and ASIC design. FPGA has many advantages over microcontroller, some of these advantages are; the speed, number of input/output ports and performance which are all very important in TLC design, at the same time ASIC design is more expensive than FPGA.

II. SURVEY ON TRAFFIC LIGHT CONTROL SYSTEM

In many cities Traffic Light Controller (TLC) is based on microcontroller and microprocessor. These TLC systems with microcontroller and microprocessor have limitations because it uses the pre-defined hardware, which is works as given program that does not have the flexibility of modification on real time basis. This program is fixed which is not reprogrammable or erasable by designer .Due to the fixed time intervals of green, orange and red signals the waiting time is more. If waiting time of vehicles is more than fuel loss also occurred. So we have to implement some advanced system for traffic control due to this road user can save their time. The implementation of traffic Light Controller can be through Application Specific Integrated Circuit. ASIC design is more expensive than FPGA. Most of the TLCs implemented on FPGA are simple ones that have been implemented as examples of FSM. Traffic Light Control System can be implemented with Programmable Logic Device (PLD) and Complex Programmable Logic Device (CPLD). PLD like PALs and GALs are available only in small sizes, equivalent to a hundred of logic gates. So traffic light control system is not controlled by PLDs which is having more crowds of vehicles on road. Complex Programmable Logic Device (CPLD) is also used for TLC system. CPLD having large number of logic gates Now, CPLD can replace thousands, or even hundreds of thousands, of logic gates. But CPLDs doesn't have much memory. Due to lack of memory devices require lots of flip flops which complicate the design of system. When comparison of response time for various frequencies, for both is observed CPLD was performing twice as better than PLD. PLD based circuit shows a delayed response.

The response with respect to clock, found that delay response of PLD is twice as much than the delay response of CPLD at a nano second level. Traffic system which requires fast response, CPLD may be the best choice. But further More to implement more complex circuits and tested the capability; the CPLD is not useful because not having very large number of gates capacity. CPLDs having thousand to ten thousand of logic gates available. FPGA is the perfect replacement for CPLD. CPLD and FPGA is having somewhat same features but FPGA is having more logic gates availability. FPGAs typically range from tens of thousands to several million which is more than CPLD.

III. FIELD PROGRAMMABLE LOGIC ARRAY

A field-programmable gate array (FPGA) is a semiconductor device that can be configured by the designer after manufacturing hence the name "field-programmable". By using a logic circuit diagram or a source code in a hardware description language (HDL) FPGAs are programmed. This program is reprogrammable by designer when it necessary .If FPGA is programmed by user then also user can edit or change the program. Implemented program in FPGA shows the working of chip or kit. They can be used to implement any logical function that an application-specific integrated circuit (ASIC) could perform, but the ability to update the functionality after shipping offers advantages for many applications. Field Programmable Gate Arrays (FPGAs) are expansively used in quick prototyping and verification of conceptual design and also used in electronic systems where the mask-production of a custom IC becomes really expensive due to the small quantity. The system has been implemented in hardware using Spartan-3E FPGA. FPGA design flow is shown in Fig1.

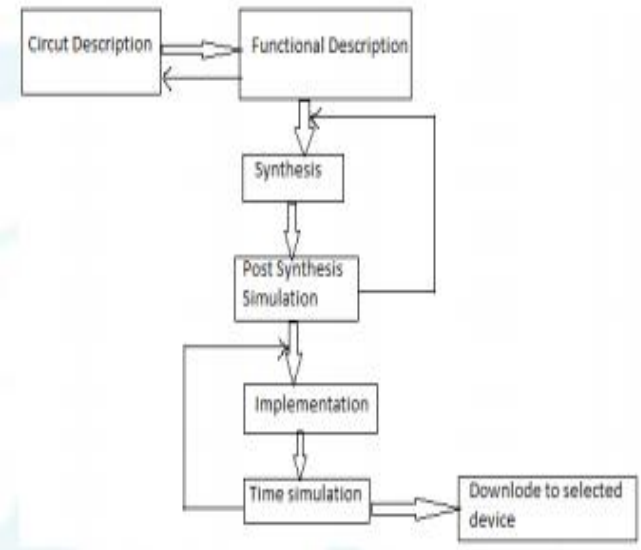

Fig.1. FPGA Design Flow.

According to that start with circuit description in which all the circuit is designed by logic gats which is done by using Hardware Description Language (HDL) .Then functional description was done which is followed synthesis and post Synthesis simulation. FPGAs have gained rapid acceptance and growth over the past decade because they can be applied to a very wide range of applications. A list of typical applications includes: random logic, integrating multiple SPLDs, device controllers, communication encoding and filtering, small to medium sized systems with SRAM blocks. Other interesting applications of FPGAs are prototyping of designs later to be implemented in gate arrays, and also emulation of entire large hardware systems.

IV. INTELLIGENT AND ADAPTIVE TRAFFIC LIGHT CONTROLLER

A. Four Road Traffic Structure

Here Ti is the traffic of ith road, e.g. Tl- traffic of 1st road, RC is Infrared sensor for activation of camera module. SS is a sound sensor for detection of emergency vehicle. For traffic T1, sensors aI, a2, a3 are installed at different distances, respectively. Similarly for traffic T2, T3 and T4 sensors installed b, c, d respectively. All these sensors are installed as per the earlier said distance of Tl traffic. Fig. 2. Shows, four way traffic with sensor module.

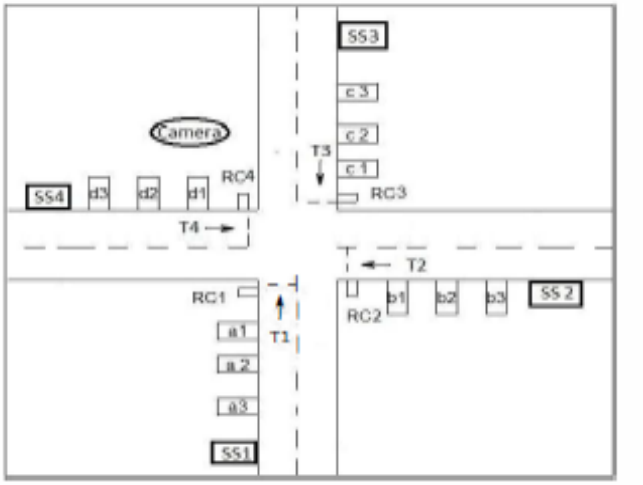

Fig.2. Four Way Traffic with Sensor Module

If any one of the road's IR sensor is sensed, respective time is given as per the no. of sensors, which sensed the input for the particular traffic to pass. But if again the same sensor senses the signal then controller checks for other roads sensor's status and provides the service accordingly. For switching of traffic lights from one state to another, following method is executed:

- When provided pass time for a particular traffic is about to finish and still vehicles are available on current traffic road then current pass signal turns red only if vehicle on other Road is sensed, otherwise current traffic road signal remains green.
- When the allotted time of a current traffic finishes and still there is no traffic on current as well as on other roads, then current traffic road signal remains green unless other roads Sense traffic.

V. STATE MACHINE, STATE TABLE

Working of IA-TLC system is given by the algorithm shown by flowchart in Fig.3

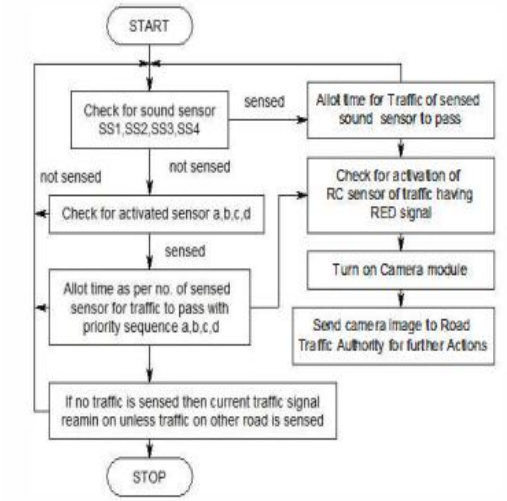

Fig.3. Flow Chart of IA-TLC.

A. State Diagram

The State diagram contains states SOS50. There will be transition from one state to other as per the traffic available on the road. State S22 is for allowing the traffic of road in which emergency vehicle is sensed, accordingly any one out of S23, S24, S25, S26, S43, S46 is executed. State Sl is executed only if no road is having emergency vehicle. State Sl checks the activated sensor with priority of checking sequence a, b, c, d, e, f and accordingly pass time is given for traffic to pass.

TABLE I

Traffic of Road	State responsible For allowing to Traffic to pass	Traffic light	Sensor status			Time alloted for Respective traffic light(SEC)
	S0	Red	If sound sensor sensed states=s22 ,otherwise s1			
	S1	Red	For a=>s2, b=>s3, c=>s4, d=>s5			
T1	S2	Red	a[2]	a[1]	a[0]	0 [Sensor a is sensed]
	S6	Green	1	0	0	6
	S7		1	1	0	12
	S8		1	1	1	15
	S9	Yellow				3
T2	S3	Red	b[2]	b[1]	b[0]	0 [Sensor b is sensed]
	S10	Green	1	0	0	6
	S11		1	1	0	12
	S12		1	1	1	15
	S13	Yellow				3
T3	S4	Red	c[2]	c[1]	c[0]	0[Sensor c is sensed]
	S14	Green	1	0	0	6
	S15		1	1	0	12
	S16		1	1	1	15
	S17	Yellow				3
T4	S5	Red	d[2]	d[1]	d[0]	0[Sensor d is sensed]
	S18	Green	1	0	0	6
	S19		1	1	0	12
	S20		1	1	1	15
	S21	Yellow				3
T5	s5	Red	e[2]	e[1]	e[0]	0[Sensor e is sensed]
	S35	Green	1	0	0	6
	S36		1	1	0	12
	S37		1	1	1	15
	S38	Yellow				3
T6	s6	Red	f[2]	f[1]	f[0]	0[Sensor f is sensed]
	S39	Green	1	0	0	6
	S40		1	1	0	12
	S41		1	1	1	15
	S42	Yellow				3

B. IR Sensor Status as Per State Table

Table I. shows an interpretation of States, Traffic of corresponding roads, sensors status, and time given for green and yellow light. If sensor al detects the traffic, al=l, Otherwise al =0. e.g. sensors a[2],a[1],a[0] are used to check the traffic intensity of road 1.

TABLE II

Traffic Pass Time with Sensors Activation

Road	State	Light	Sound sensor	Time
T1	S22	Red	Ss1=1	
	S31	Red		3
	S27	Yellow		4
	S23	Green		15
T2	S32	Red	Ss2=1	3
	S28	Yellow		4
	S24	Green		15
T3	S33	Red	Ss3=1	3
	S29	Yellow		4
	S25	Green		15
T4	S34	Red	Ss4=1	3
	S30	Yellow		4
	S26	Green		15
T5	S45	Red	Ss5=1	3
	S44	Yellow		4
	S43	Green		15
T6	S48	Red	Ss6=1	3
	S47	Yellow		4
	S46	Green		15

C. Provision of allowing Emergency Vehicles

It is our social responsibility to allow the emergency vehicle to pass first. But sometimes the emergency vehicles get stuck in the traffic jams or they have to wait in a queue till they are allowed to pass. Here an emergency vehicle is detected by using the sound sensors (ss1, ss2, ss3, ss4, ss5, and ss6). According to the signal sensed by the sound sensor, controller checks whether the detected sound signal is from the same road and then allows the traffic to flow until emergency vehicle has passed. Otherwise allow the traffic of road in which emergency Vehicle is in queue to pass, blocking other traffic. After passing of emergency vehicle default sequence of traffic flow continues.

D. Camera module

When the allowed traffic is passing that is respective RC sensor senses logic 1 and remaining RC sensor receives logic 0, then logic 0 is provided to the camera and camera is in ideal position. If along with the allowed traffic, traffic of a restricted road is trying to cross the respective RC sensor then logic 1 is provided to camera module and it captures images, which are forwarded to Road Traffic Authority for further action.

VI. SIMULATION RESULTS

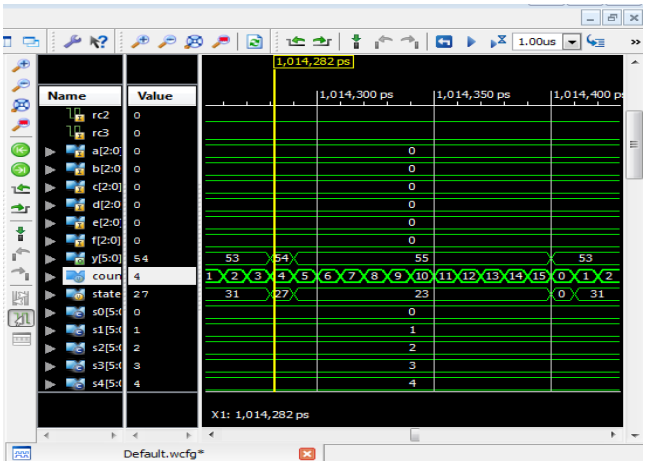

Fig.4.

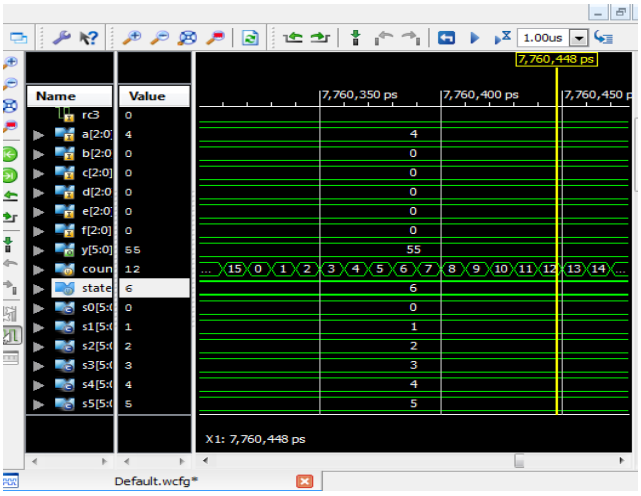

Fig.5.

VII. CONCLUSION

The modern ways of multi-way traffic management improves the traffic condition up to a large extent. Traffic intensity is sensed and accordingly time is allotted for traffic to pass. The main feature of this study is the dynamic traffic pass time allocation and provision to detect the emergency vehicles like ambulance, fire brigade etc, giving them priority to pass first and then traffic resumes normally. Camera module is used to find the defaulter for crossing the red signal by means of sensors. This Design works with same efficiency at day and night time due to installation of IR sensors for providing dynamic traffic time.Verilog HDL is used to circuit description, code is generated which is simulated using xilinx14.3.

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