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Ultra Low Power Design of Sequential Logic Circuits using Adiabatic Logic

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Abstract: Demand for the design of low power consumption circuits is increasing, in view of that, new methodologies been invented for the design of low power consumption devices. Now a day's every electronic equipment is battery powered, power consumption of the elements must be reduced to run the electronic devices for long time. There are several techniques for the low power design of circuits among that, adiabatic logic technique is one of the best. In this we are discussing about Modified positive feedback adiabatic logic which will have less power consumption compared to existing adiabatic techniques. In this a linear feedback shift register is designed with modified positive feedback adiabatic logic using Mentor Graphics Tool.

Keywords: Adiabatic Logic, PFAL, Modified PFAL.

I. INTRODUCTION

Adiabatic circuits are low power hardware which utilizes "reversible logic" to save energy. The word adiabatic‖ originates from a Greek word that portrays thermodynamic procedures which exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat[1]. In perfect adiabatic logic, every charge could be recycled (reused) a limitless number of times. So that a huge power dissipation lessening would be conceivable. Progressively figuring, such perfect process can't be accomplished as a result of the nearness of dissipative components like resistances in a circuit[2]. There are established ways to deal with decrease the dynamic power, for example, lessening supply voltage, diminishing physical capacitance and decreasing switching activity. Adiabatic logic chips away at the idea of switching exercises which decreases the power by giving put away energy back to the supply[3]. There are a few rules that are shared by all of these low - power adiabatic systems. These incorporate just turning switches on when there is no potential difference crosswise over them, just turning switches off when no current is flowing through them, and utilizing a power supply that is prepared to do recouping or reusing vitality as electric charge[4]. To accomplish this, when all is said in done, the power supplies of adiabatic logic circuits have utilized steady current charging , as opposed to more conventional non-adiabatic systems that have for the most part utilized consistent voltage charging from a fixed-voltage power supply[5] .The power supplies of adiabatic logic circuits have likewise utilized circuit components fit for putting away vitality[6].

This is regularly done utilizing inductors which store the vitality by changing over it to attractive flux, or utilizing capacitors, which can specifically store electric charge[7]. There are various equivalent words that have been utilized by different creators to allude to adiabatic logic sort systems, these include: ―Charge recovery logic‖ ,―Charge recycling logic‖, ―Clock-powered logic‖, ―Energy recovery logic‖ and ―Energy recycling logic. On account of the reversibility necessities for a framework to be completely adiabatic, a large portion of these equivalent words really allude to, and can be utilized between variably, to depict semi adiabatic systems.[8][9]

- Adiabatic logics are of two main types. They are:
- Partially adiabatic logic.
- Fully adiabatic logic.

Now, partially adiabatic logic is a logic having non-adiabatic loss present i.e. there is non -zero V_{DS} across transistor when it is being turned ON. It doesn't depend upon frequency. It can be further classified as:

- Efficient charge recovery logic (ECRL).
- 2N-2N 2P logic.
- Positive feedback adiabatic logic (PFAL).
- NMOS energy recovery logic (NERL).
- Clocked adiabatic logic (CAL).

Fully adiabatic logic is a logic having non -adiabatic loss absent . It depends upon frequency. It can be classified as:

- Pass transistor adiabatic logic.
- Split rail charge recovery logic. (SCRL)

A. Positive Feedback Adiabatic Logic

The partial energy recovery circuit structure named Positive Feedback Adiabatic Logic (PFAL) has been utilized, since it demonstrates the most minimal energy consumption if contrasted with other comparable families, and a decent robustness against technological parameter variations[10]. It is a dual-rail circuit with partial energy recovery[11] .The general schematic of the PFAL entryway is shown in Figure

1. The center of all the PFAL entryways is an adiabatic amplifier, a hook made by the two PMOS and two NMOS, that keeps away from a logic level degradation on the output nodes out and /out. The two n-trees understand the logic functions. This logic family additionally generates both positive and negative outputs.[12]

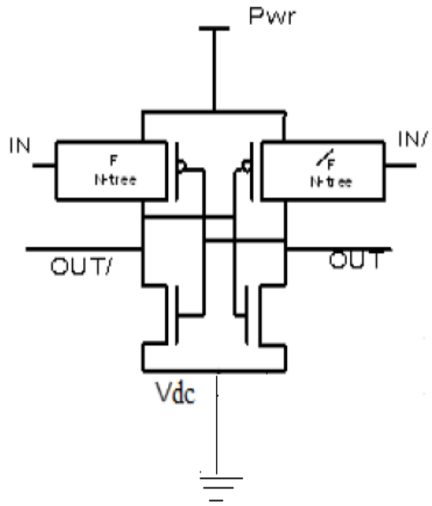

Fig.1. Basic Structure of Positive Feedback Adiabatic Logic (PFAL) Inverter

B. Modified Positive Feedback Adiabatic Logic

The circuit diagram for modified PFAL adiabatic circuit is shown in Fig2.It implements basic Inverter functionality[13]. It uses an additional drain gate connected NMOS transistor, in between the source and ground terminal of PFAL cross-coupled inverters to reduce the power dissipation more than PFAL inverter design[14].

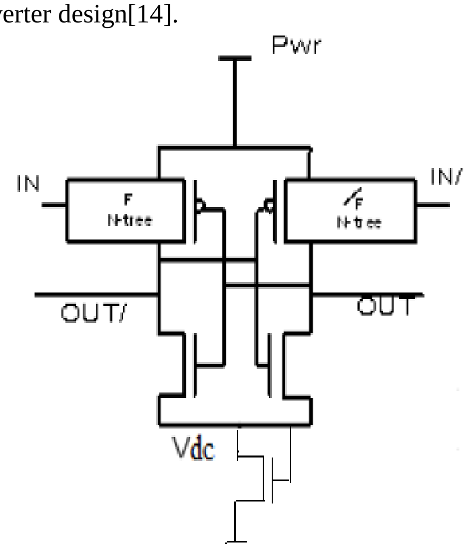

Fig.2. MPFAL Inverter

C. Flip Flop

The below figure shows the schematic diagram of d-ff using mpfal technique, this is having two inputs. One input is given as binary 1 or 0 and another i/p as clock signal.

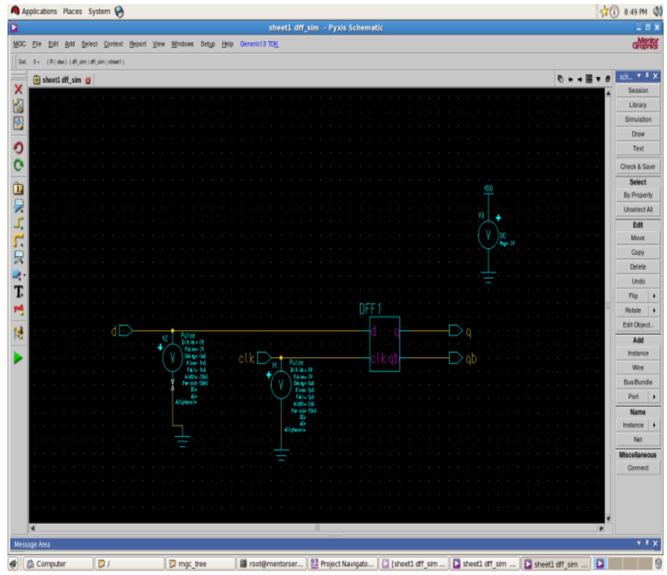

Fig.3. Schematic Diagram of D-FF

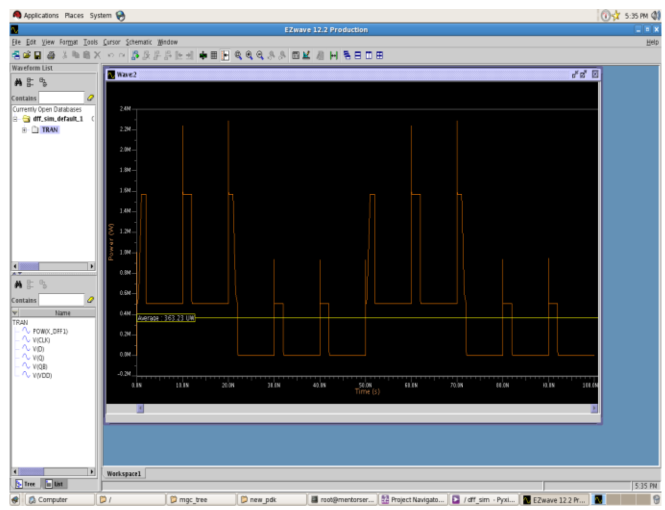

Fig.4. Simulation Results of D-FF.

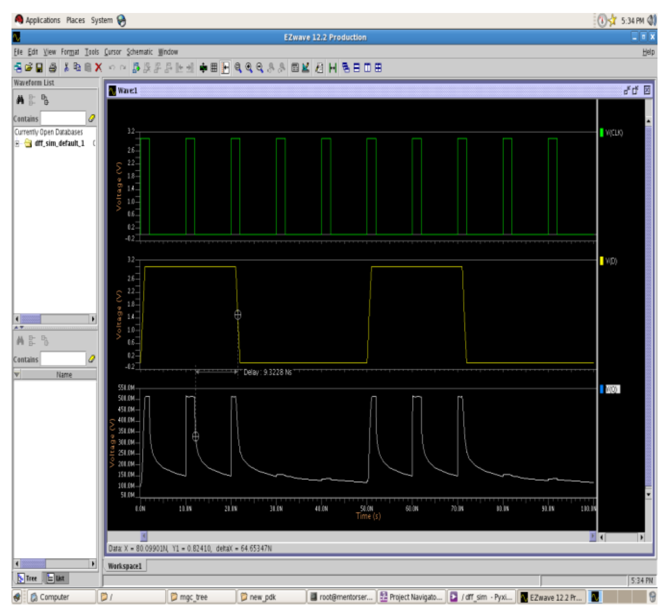

Fig.5. Simulation Results of D-FF.

D. Linear Feed Back Shift Register

Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of D flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. All the flip-flops are driven by a common clock, and all are set or reset simultaneously. [15][16] Shift registers can be classified according to the way the input data are read in and the way the output data are readout. There are four types of shift registers:

1. Serial-In-Serial-Out.
2. Serial-In-Parallel-Out.
3. Parallel-In-Serial-Out.
4. Parallel-In-Parallel-Out.

1. Serial-In-Serial-Out Shift Register

A basic Serial-In-Serial-Out four-bit shift register can be constructed using four D flip-flops, as shown in Figure 6. The operation of the circuit is as follows:

- The register is first cleared, forcing all four outputs of the flip flops to zero.
- The input data is then applied sequentially to the D input of the first flip-flop on the left (FF0).
- During each clock pulse, one bit is transmitted from left to right. Assume a data word to be 1001. The least significant bit of the data has to be shifted through the register from FF0 to FF3.

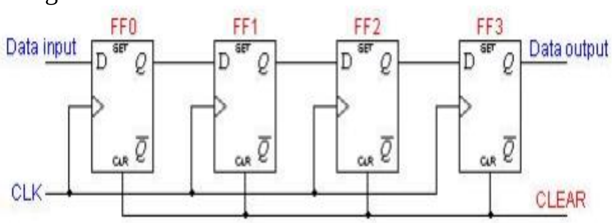

Fig.6. Serial in Serial Out Shift Register

2. Serial-In-Parallel-Out Shift Register

In this type of registers, data bits are entered serially, but outputs are obtained simultaneously from each flip-flop. Once the data are stored, each bit appears on its respective output line, and all bits are available at the same time. The construction of a four-bit Serial-In-Parallel-Out shift register is shown in Figure

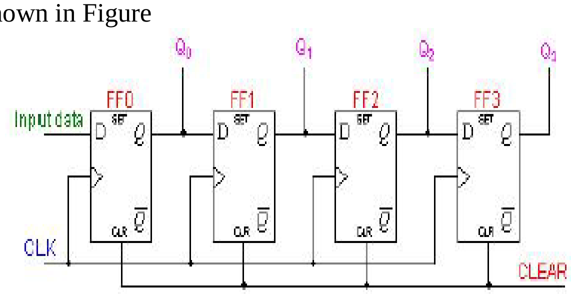

Fig.7. Serial-In-Parallel-Out shift register

3. Parallel-In-Serial-Out Shift Register

In Parallel-in-Serial-Out shift register, all data bits are available at the shift register inputs simultaneously but are read out in series (bit by bit). Figure 2.13 shows a Parallel-in-Serial-Out shift register. The *write / shift* input will determine wither that parallel data is being readin o r the data is being shifted in series. If *write / shift* is 0, then the data is written to the register in parallel (simultaneously). If *write / shift* is 1, the data is shifted in series and the output is read at Q3.

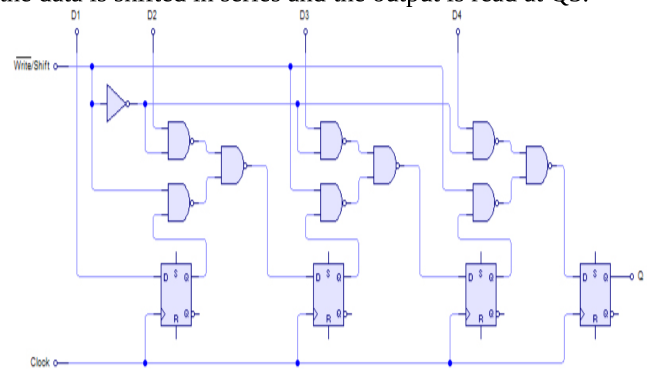

Fig.8. Parallel-In-Serial-Out Shift Register

4. Parallel-In-Parallel-Out Shift Register

For Parallel-in-Parallel-Out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a four-bit Parallel-in-Parallel-Out shift register constructed using D flip-flops.

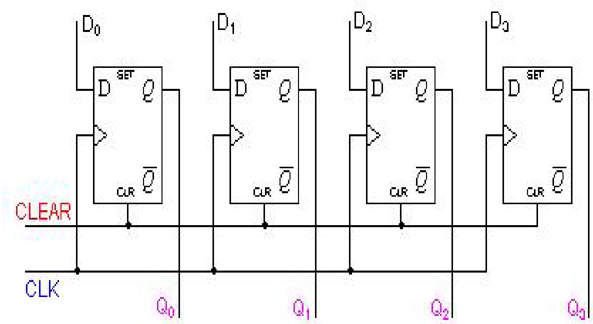

Fig.9. Parallel-In-Parallel-Out Shift Register

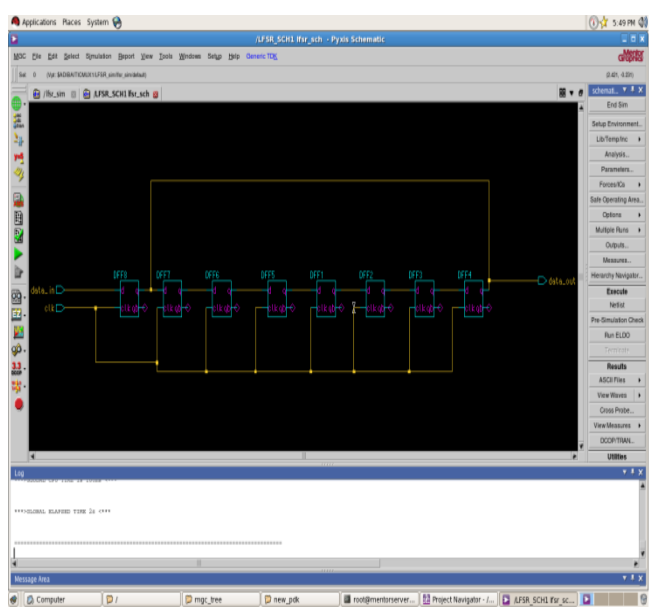

Fig.10. Schematic Diagram of LFSR –SISO

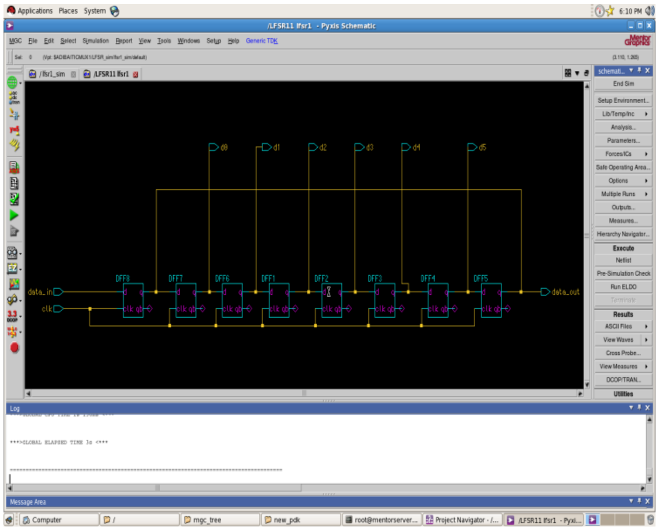

Fig.11. Schematic Diagram of LFSR-SIPO

II. RESULTS&DISCUSSIONS

The design of linear feedback shift register using modified feedback adiabatic logic is done using mentor graphics tool. The power consumption is very less compared to the design using CMOS technology. The power consumption of D-FF design using modified feedback adiabatic logic is 363.23uw and The power consumption of 8 bit linear feedback shift register is 1.2mw. further the design can be extended to large circuits such as multiplexers, encoders, decoders etc.

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