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Implementation High-Level Syntax Architecture for Efficient Integer DCT for HEVC

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Abstract: In this paper, we present High Efficiency Video Coding (HEVC) inverse transform for residual coding uses 2-D 4x4 to 32x32 transforms with higher precision as compared to H.264/AVC's 4x4 and 8x8 transforms resulting in an increased hardware complexity. In this paper, an energy and area efficient VLSI architecture of an HEVC-compliant inverse transform and dequantization engine is presented. We implement a pipelining scheme to process all transform sizes at a minimum throughput of 2 pixel/cycle with zero-column skipping for improved throughput. We use data gating in the 1-D Inverse Discrete Cosine Transform engine to improve energy-efficiency for smaller transform sizes. A high-density SRAM-based transpose memory is used for an area-efficient design. This design supports decoding of 4K Ultra-HD (3840x2160) video at 30 frame/sec. The inverse transform engine takes 98.1 kgate logic, 16.4 Kbit SRAM and 10.82 pJ/pixel while the dequantization engine takes 27.7 kgate logic, 8.2 Kbit SRAM and 1.10 pJ/pixel in 40 nm CMOS technology. Although larger transforms require more computation per coefficient, they typically contain a smaller proportion of non-zero coefficients. Due to this trade-off, larger transforms can be more energy-efficient. The proposed architecture is found to support ultrahigh definition 7680×4320 at 60 frames/s video, which is one of the applications of HEVC.

Keywords: Discrete Cosine Transforms (DCT), H.265, High Efficiency Video Coding (HEVC), Integer Discrete Cosine Transform (DCT), Video Coding.

I. INTRODUCTION

The High Efficiency Video Coding (HEVC) standard is the most recent joint video project of the ITU-T Video Coding Experts Group (VCEG) and the ISO/IEC Moving Picture Experts Group (MPEG) standardization organizations, working together in a partnership known as the Joint Collaborative Team on Video Coding (JCTVC). The first edition of the HEVC standard is expected to be finalized in January 2013, resulting in an aligned text that will be published by both ITU-T and ISO/IEC. Additional work is planned to extend the standard to support several additional application scenarios, including extended-range uses with enhanced precision and color format support, scalable video coding, and 3-D/stereo/multi-view video coding. In ISO/IEC, the HEVC standard will become MPEG-H Part 2 (ISO/IEC 23008-2) and in ITU-T it is likely to become ITU-T Recommendation H.265. Video coding standards have evolved primarily through the development of the well-known ITUT and ISO/IEC standards. The ITU-T produced H.261 and H.263, ISO/IEC produced MPEG-1 and MPEG-4 Visual, and the two organizations jointly produced the H.262/MPEG-2 Video and H.264/MPEG-4 Advanced Video Coding (AVC) standards. The two standards that were jointly produced have had a particularly strong impact and have found their way into a wide variety of products that are increasingly prevalent in our daily lives.

Throughout this evolution, continued efforts have been made to maximize compression capability and improve other characteristics such as data loss robustness, while considering the computational resources that were practical for use in products at the time of anticipated deployment of each standard. The Discrete cosine transform (DCT) plays a vital role in video compression due to its near optimal de correlation efficiency. Several variations of integer DCT have been suggested in the last two decades to reduce the computational complexity. The new H.265/High Efficiency Video Coding (HEVC) standard has been recently finalized and poised to replace H.264/AVC. Some hardware architectures for the integer DCT for HEVC have also been proposed for its real time implementation decomposed the DCT matrices into sparse sub matrices where the multiplications are avoided by using the lifting scheme used the multiplier less multiple constant multiplication (MCM) approach for four-point and eight-point DCT, and have used the normal multipliers with sharing techniques for 16 and 32-point DCTs have used Chen's factorization of DCT where the butterfly operation has been implemented by the processing element with only shifters, adders, and multiplexors proposed a unified structure to be used for forward as well as inverse transform after the matrix decomposition.

One key feature of HEVC is that it supports DCT of different sizes such as 4, 8, 16, and 32. Therefore, the hardware architecture should be flexible enough for the computation of DCT of any of these lengths. The existing designs for conventional DCT based on constant matrix multiplication (CMM) and MCM can provide optimal solutions for the computation of any of these lengths, but they are not reusable for any length to support the same throughput processing of DCT of different transform lengths. Considering this issue, we have analyzed the possible implementations of integer DCT for HEVC in the context of resource requirement and reusability, and based on that, we have derived the proposed algorithm for hardware implementation. We have designed scalable and reusable architectures for 1-D and 2-D integer DCTs for HEVC that could be reused for any of the prescribed lengths with the same throughput of processing irrespective of transform size. In the next section, we present HEVC Coding Design and Feature Highlights. In Section III, High-Level Syntax Architecture. In Section IV, we propose power-efficient designs of transposition buffers for full-parallel and folded implementations of 2-D Integer DCT. In Section IV, we compare the synthesis result of the proposed architecture with those of existing architectures for HEVC finally Section V gives conclusion of this paper.

II. HEVC CODING DESIGN AND FEATURE HIGHLIGHTS

The HEVC standard is designed to achieve multiple goals, including coding efficiency, ease of transport system integration and data loss resilience, as well as implement ability using parallel processing architectures. The following subsections briefly describe the key elements of the design by which these goals are achieved, and the typical encoder operation that would generate a valid bit stream.

A. Video Coding Layer

The video coding layer of HEVC employs the same hybrid approach (inter-/intra-picture prediction and 2-D transform coding) used in all video compression standards since H.261. Fig.1 depicts the block diagram of a hybrid video encoder, which could create a bit stream conforming to the HEVC standard. An encoding algorithm producing an HEVC compliant bit stream would typically proceed as follows. Each picture is split into block-shaped regions, with the exact block partitioning being conveyed to the decoder. The first picture of a video sequence (and the first picture at each clean random access point into a video sequence) is coded using only intra-picture prediction (that uses some prediction of data spatially from region-to-region within the same picture, but has no dependence on other pictures). For all remaining pictures of a sequence or between random access points, inter-picture temporally predictive coding mode is typically used for most blocks. The encoding process for inter-picture prediction consists of choosing motion data comprising the selected reference picture and motion vector (MV) to be applied for predicting the samples of each block. The encoder and decoder generate identical inter-picture prediction signals by applying motion compensation (MC) using the MV and mode decision data, which are transmitted as side information.

The residual signal of the intra- or inter-picture prediction, which is the difference between the original block and its prediction, is transformed by a linear spatial transform. The transform coefficients are then scaled, quantized, entropy coded, and transmitted together with the prediction information. The encoder duplicates the decoder processing loop (see gray-shaded boxes in Fig. 1) such that both will generate identical predictions for subsequent data. Therefore, the quantized transform coefficients are constructed by inverse scaling and are then inverse transformed to duplicate the decoded approximation of the residual signal. The residual is then added to the prediction, and the result of that addition may then be fed into one or two loop filters to smooth out artifacts induced by block-wise processing and quantization. The final picture representation (that is a duplicate of the output of the decoder) is stored in a decoded picture buffer to be used for the prediction of subsequent pictures. In general, the order of encoding or decoding processing of pictures often differs from the order in which they arrive from the source; necessitating a distinction between the decoding order (i.e., bit-stream order) and the output order (i.e., display order) for a decoder.

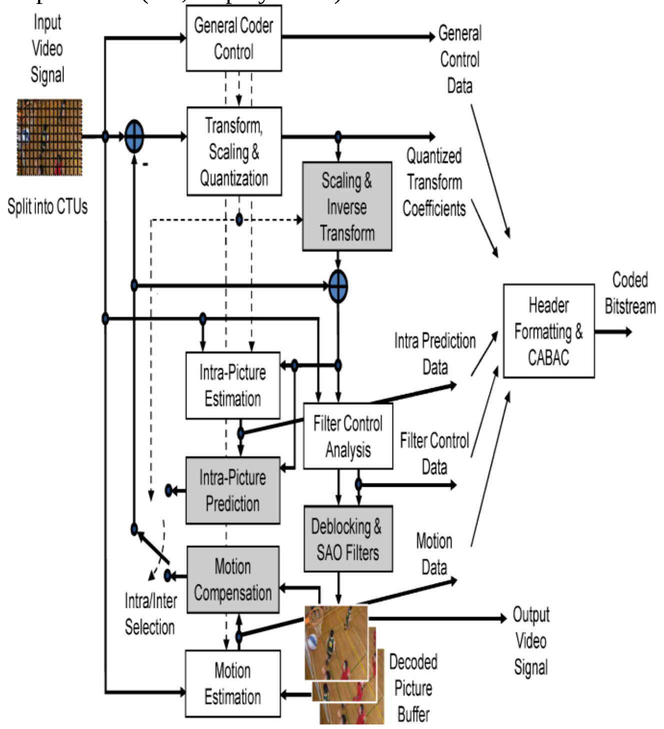

Fig.1. Typical HEVC video encoder (with decoder modeling elements shaded in light gray).

Video material to be encoded by HEVC is generally expected to be input as progressive scan imagery (either due to the source video originating in that format or resulting from de-interlacing prior to encoding). No explicit coding features are present in the HEVC design to support the use of interlaced scanning, as interlaced scanning is no longer used for displays and is becoming substantially less common for distribution. However, metadata syntax has been provided in HEVC to allow an encoder to indicate that interlace-scanned video has been sent by coding each field (i.e., the even or odd numbered lines of each video frame) of interlaced video as a separate picture or that it has been sent by coding each interlaced frame as an HEVC coded picture. This provides an efficient method of coding interlaced video without burdening decoders with a need to support a special decoding process for it. In the following, the various features involved in hybrid video coding using HEVC are highlighted as follows.

1. Coding Tree Units And Coding Tree Block (CTb) Structure: The core of the coding layer in previous standards was the macro-block, containing a 16×16 block of luma samples and, in the usual case of 4:2:0 color sampling, two corresponding 8×8 blocks of chroma samples; whereas the analogous structure in HEVC is the coding tree unit (CTU), which has a size selected by the encoder and can be larger than a traditional macro-block. The CTU consists of a luma CTB and the corresponding chroma CTBs and syntax elements. The size L×L of a luma CTB can be chosen as L = 16, 32, or 64 samples, with the larger sizes typically enabling better compression. HEVC then supports a partitioning of the CTBs into smaller blocks using a tree structure and quad-tree-like signaling.

2. Coding Units (CUs) and Coding Blocks (CBs): The quad tree syntax of the CTU specifies the size and positions of its luma and chroma CBs. The root of the quad-tree is associated with the CTU. Hence, the size of the luma CTB is the largest supported size for a luma CB. The splitting of a CTU into luma and chroma CBs is signaled jointly. One luma CB and ordinarily two chroma CBs, together with associated syntax, form a coding unit (CU). A CTB may contain only one CU or may be split to form multiple CUs, and each CU has an associated partitioning into prediction units (PUs) and a tree of transform units (TUs).

3. Prediction Units and Prediction Blocks (PBs): The decision whether to code a picture area using inter-picture or intra-picture prediction is made at the CU level. A PU partitioning structure has its root at the CU level. Depending on the basic prediction-type decision, the luma and chroma CBs can then be further split in size and predicted from luma and chroma prediction blocks (PBs). HEVC supports variable PB sizes from 64×64 down to 4×4 samples.

4. TUs and Transform Blocks: The prediction residual is coded using block transforms. A TU tree structure has its root at the CU level. The luma CB residual may be identical to the luma transform block (TB) or may be further split into smaller luma TBs. The same applies to the chroma TBs. Integer basis functions similar to those of a discrete cosine transform (DCT) are defined for the square TB sizes 4×4, 8×8, 16×16, and 32×32. For the 4×4 transform of luma intra-picture prediction residuals, an integer transform derived from a form of discrete sine transform (DST) is alternatively specified.

5. Motion Vector Signaling: Advanced motion vector prediction (AMVP) is used, including derivation of several most probable candidates based on data from adjacent PBs and the reference picture. A merge mode for MV coding can also be used, allowing the inheritance of MVs from temporally or spatially neighboring PBs. Moreover, compared to H.264/MPEG-4 AVC, improved skipped and direct motion inference is also specified.

6. Motion Compensation: Quarter-sample precision is used for the MVs, and 7-tap or 8-tap filters are used for interpolation of fractional-sample positions (compared to six-tap filtering of half-sample positions followed by linear interpolation for quarter-sample positions in H.264/MPEG-4 AVC). Similar to H.264/MPEG-4 AVC, multiple reference pictures are used. For each PB, either one or two motion vectors can be transmitted, resulting either in uni-predictive or bi-predictive coding, respectively. As in H.264/MPEG-4 AVC, a scaling and offset operation may be applied to the prediction signal(s) in a manner known as weighted prediction.

7. Intra Picture Prediction: The decoded boundary samples of adjacent blocks are used as reference data for spatial prediction in regions where inter picture prediction is not performed. Intra picture prediction supports 33 directional modes (compared to eight such modes inH.264/MPEG-4 AVC), plus planar (surface fitting) and DC (flat) prediction modes. The selected intra picture prediction modes are encoded by deriving most probable modes (e.g., prediction directions) based on those of previously decoded neighboring PBs.

8. Quantization Control: As in H.264/MPEG-4 AVC, uniform reconstruction quantization (URQ) is used in HEVC, with quantization scaling matrices supported for the various transform block sizes.

9. Entropy Coding: Context adaptive binary arithmetic coding (CABAC) is used for entropy coding. This is similar to the CABAC scheme in H.264/MPEG-4 AVC, but has undergone several improvements to improve its throughput speed (especially for parallel-processing architectures) and its compression performance, and to reduce its context memory requirements.

10. In-Loop De-Blocking Filtering: A de-blocking filter similar to the one used in H.264/MPEG-4 AVC is operated within the inter-picture prediction loop. However, the design is simplified in regard to its decision-making and filtering processes, and is made friendlier to parallel processing.

11. Sample Adaptive Offset (SAO): A nonlinear amplitude mapping is introduced within the inter-picture prediction loop after the de-blocking filter. Its goal is to better reconstruct the original signal amplitudes by using a look-up table that is described by a few additional parameters that can be determined by histogram analysis at the encoder side.

III. HIGH-LEVEL SYNTAX ARCHITECTURE

A number of design aspects new to the HEVC standard improve flexibility for operation over a variety of applications and network environments and improve robustness to data losses. However, the high-level syntax architecture used in the H.264/MPEG-4 AVC standard has generally been retained, including the following features.

- **Parameter set structure:** Parameter sets contain information that can be shared for the decoding of several regions of the decoded video. The parameter set structure provides a robust mechanism for conveying data that are essential to the decoding process. The concepts of sequence and picture parameter sets from H.264/MPEG-4 AVC are augmented by a new video parameter set (VPS) structure.
- **NAL unit syntax structure:** Each syntax structure is placed into a logical data packet called a network abstraction layer (NAL) unit. Using the content of a two byte NAL unit header, it is possible to readily identify the purpose of the associated payload data.
- **Slices:** A slice is a data structure that can be decoded independently from other slices of the same picture, in terms of entropy coding, signal prediction, and residual signal reconstruction. A slice can either be an entire picture or a region of a picture. One of the main purposes of slices is resynchronization in the event of data losses. In the case of packetized transmission, the maximum number of payload bits within a slice is typically restricted, and the number of CTUs in the slice is often varied to minimize the packetization overhead while keeping the size of each packet within this bound.
- **Supplemental enhancement information (SEI) and video usability information (VUI) metadata:** The syntax includes support for various types of metadata known as SEI and VUI. Such data provide information about the timing of the video pictures, the proper interpretation of the color space used in the video signal, 3-D stereoscopic frame packing information, other display hint information, and so on.

A. Parallel Decoding Syntax and Modified Slice Structuring

Finally, four new features are introduced in the HEVC standard to enhance the parallel processing capability or modify the structuring of slice data for packetization purposes. Each of them may have benefits in particular application contexts, and it is generally up to the implementer of an encoder or decoder to determine whether and how to take advantage of these features.

1. Tiles: The option to partition a picture into rectangular regions called tiles has been specified. The main purpose of tiles is to increase the capability for parallel processing rather than provide error resilience. Tiles are independently decodable regions of a picture that are encoded with some shared header information. Tiles can additionally be used for the purpose of spatial random access to local regions of video pictures. A typical tile configuration of a picture consists of segmenting the picture into rectangular regions with approximately equal numbers of CTUs in each tile. Tiles provide parallelism at a more coarse level of granularity (picture/sub picture), and no sophisticated synchronization of threads is necessary for their use.

2. Wave Front Parallel Processing: When wave front parallel processing (WPP) is enabled, a slice is divided into rows of CTUs. The first row is processed in an ordinary way, the second row can begin to be processed after only two CTUs have been processed in the first row, and the third row can begin to be processed after only two CTUs have been processed in the second row, and so on. The context models of the entropy coder in each row are inferred from those in the preceding row with a two-CTU processing lag. WPP provides a form of processing parallelism at a rather fine level of granularity, i.e., within a slice. WPP may often provide better compression performance than tiles (and avoid some visual artifacts that may be induced by using tiles).

3. Dependent Slice Segments: A structure called a dependent slice segment allows data associated with a particular wave front entry point or tile to be carried in a separate NAL unit, and thus potentially makes that data available to a system for fragmented packetization with lower latency than if it were all coded together in one slice. A dependent slice segment for a wave front entry point can only be decoded after at least part of the decoding process of another slice segment has been performed. Dependent slice segments are mainly useful in low-delay encoding, where other parallel tools might penalize compression performance.

VI. IMPLEMENTATION RESULTS AND DISCUSSIONS

A. Synthesis Results of 1-D Integer DCT

We have coded the architecture derived from the reference algorithm as well as the proposed architectures for different transform lengths in VHDL, and synthesized by Synopsys Design Compiler using TSMC 90-nm General Purpose (GP) CMOS Library. The word lengths of input samples are chosen to be 16 bits. The area, computation time, and power consumption (at 100-MHz clock frequency) obtained from the synthesis reports are shown in Table I. It is found that the proposed architecture involves nearly 14% less are a delay product (ADP) and 19% less energy per sample (EPS) compared to the direct implementation of reference algorithm, in average, for integer DCT of lengths 4, 8, 16, and 32. Additional 19% saving in ADP and 20% saving in EPS are also achieved by the pruning scheme with nearly the same throughput rate. The pruning scheme is more effective for higher length DCT since the percentage of total area occupied by the SAUs increases as DCT length increases, and hence more adders are affected by the pruning scheme.

B. Comparison with the Existing Architectures

We have named the proposed reusable integer DCT architecture before applying pruning as reusable architecture-1 and that after applying pruning as reusable architecture-2. The processing rate of the proposed integer DCT unit is 16 pixels per cycle considering 2-D folded structure since 2-D transform of 32 × 32 block can be obtained in 64 cycles. In order to support 8K ultrahigh definition (UHD) (7680 × 4320) at 30 frames/s and 4:2:0 YUV format that is one of the applications of HEVC, the proposed reusable architectures should work at the operating frequency faster than 94 MHz (7680 ×4320 ×30 ×1.5/16). The computation times of 5.56 ns and 5.27 ns for reusable architectures-1 and 2, respectively (obtained from the synthesis without any timing constraint) are enough for this application. Also, the computation time less than 5.358 ns is needed to support 8K UHD at 60 frames/s, which can be achieved by slight increase in silicon area when we synthesize the reusable architecture-1 with the desired timing constraint. Table II lists the synthesis results of the proposed reusable architectures, as well as the existing architectures for HEVC for N = 32 in terms of gate count that is normalized by area of 2-input NAND gate, maximum operating frequency, processing rate, throughput, and supporting video format.

TABLE I: Area, Time, and Power Complexities of Proposed Architectures and Direct Implementation of Reference Algorithm of Integer DCT for Various Lengths Based on Synthesis Result Using TSMC 90-nm CMOS Library

Design		Area Consumption	Computation Time	Power Consumption	Area-Delay Product	Energy per Sample	Excess Area-Delay Product	Excess Energy per Sample
Architecture	N							
Using Reference Algorithm	4	4656	2.84	0.28	13223	0.68	18.95%	27.18%
	8	21457	3.25	1.68	69735	2.01	51.23%	59.03%
	16	88451	3.67	7.45	324615	4.48	57.79%	67.20%
	32	332889	3.96	29.75	1318240	8.96	51.06%	68.66%
Proposed Algorithm Before Pruning	4	4399	2.95	0.26	12977	0.63	16.73%	17.10%
	8	16772	3.34	1.31	56018	1.57	21.48%	24.02%
	16	66130	3.92	5.73	259229	3.45	26.00%	28.77%
	32	253432	4.48	23.17	1135375	6.98	30.10%	31.46%
Proposed Algorithm After Pruning	4	3794	2.93	0.22	11116	0.54	--	--
	8	13931	3.31	1.06	46111	1.26	--	--
	16	52480	3.92	4.45	205721	2.68	--	--
	32	196103	4.45	17.63	872658	5.31	--	--

The proposed reusable architecture-2 requires larger area than the design of [12], but offers much higher throughput. Also, the proposed architectures involve less gate counts, as well as higher throughput, than the design of [11]. Specially, the designs of [11] and [12] require very high operational frequencies of 761 MHz and 1403 MHz in order to support UHD at 60 frames/s since 2-D transform of 32×32 block can be computed in 261 cycles and 481 cycles, respectively. However, 187 MHz operating frequency that is needed to support 8K UHD at 60 frames/s by the proposed architecture can be obtained using TSMC 90-nm or newer technologies as shown in Table II. Also, we could obtain the frequency of 94 MHz for UHD at 30 frames/s and 4:2:0 YUV format using TSMC 0.15-μm or newer technologies.

TABLE II: Comparison of Different 1-D Integer DCT Architectures with the Proposed Architectures

Design	Technology	Gate Counts	Max Freq.	Pixels/Cycle	Throughput	Supporting Video Format
Shen et al [10]	0.13-μm	134 K	350 MHz	4	1.40 Gsps	4096x2048 @ 30 fps
Park et al [11]	0.18-μm	52 K	300 MHz	2.12	0.63 Gsps	3840x2160 @ 30 fps
Reusable Architecture-1	90-nm	131 K	187 MHz	16	2.99 Gsps	7680x4320 @ 60 fps
Reusable Architecture-2	90-nm	103 K	187 MHz	16	2.99 Gsps	7680x4320 @ 60 fps

TABLE III: 2-D Integer Transform With Folded Structure and Full-Parallel Structure

Architecture	Folded	Full-parallel
Technology	TSMC 90-nm GP CMOS	
Total Gate Counts	208 K	347 K
Operating Frequency	187 MHz	
Processing Rate (pels/cycle)	16	32
Throughput	2.992 G	5.984 G
Total Power Consumption	40.04 mW	67.57 mW
Energy per Sample (EPS)	13.38 pJ	11.29 pJ

C. Synthesis Results of 2-D Integer DCT

We also synthesized the folded and full-parallel structures for 2-D integer DCT. We have listed total gate counts, processing rate, throughput, power consumption, and EPS in Table III. We set the operational frequency to 187 MHz for both cases to support UHD at 60 frames/s. The 2-D full-parallel structure yields 32 samples in each cycle after initial latency of 32 cycles providing double the throughput of the folded structure. However, the full-parallel architecture consumes 1.69 times more power than the folded architecture since it has two 1-D DCT units and nearly the same complexity of transposition buffer while the throughput of full-parallel design is double the throughput of folded design. Thus, the full-parallel design involves 15.6% less EPS.

V. CONCLUSION

In this paper, we presented the hardware design of an HEVC compliant inverse transform engine capable of processing 4K Ultra-HD 30 frames/sec video in 40 nm technology. A pipelining scheme is developed to manage all TU sizes in HEVC at a worst-case throughput of 2 pixel/cycle. Zero column skipping reduces cycle-count by 27%-66% over the worst case. The design of a transpose memory using a combination of SRAM for high density and registers for high throughput is explained. Finally, a dequantization engine for all scaling list types is briefly described. This design takes 126 k gates of logic and consumes 7.8 mW of power (or 11.9 pJ/pixel). Data and explicit clock-gating improves the energy efficiency of the shared transform logic. From the synthesis result, it is found that the proposed algorithm with pruning involves nearly 30% less ADP and 35% less EPS compared to the reference algorithm in average for integer DCT of lengths 4, 8, 16, and 32 with nearly the same throughput rate.

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