FPGA Implementation of Digital Down Converter

YAMUANA K H¹, B. RAMESH NAIR²
¹ PG Scholar, Dept of ECE, Seshachala Institute of Technology, Puttur, AP, India, E-mail: yamu.rygh@gmail.com.
² Assistant Professor, Dept of ECE, Seshachala Institute of Technology, Puttur, AP, India.

Abstract: In telecommunication, a communications system is a collection of individual communications networks, transmission systems, relay stations, tributary stations, and data terminal equipment usually capable of interconnection and interoperation to form an integrated whole. The components of a communications system serve a common purpose, are technically compatible, use common procedures, respond to controls, and operate in union. Telecommunications is a method of communication. Digital down Converter has been discussed. Though the received signal is RF signal with high data rates an IF stage is used to frequency shift the signal to fixed IF which is the input to ADC. This is sampled and given as input to DDC. Signal extraction using DDC is presented in detail. It is shown that filter bandwidth varies by varies with decimation factor. Decimation range in this paper is 2 to 16384. Filtering is implemented in stages to obtain efficient response. Also, the reasons for choosing FPGA over ASSP’s to implement DDC are provided. Xilinx ISE 10.1 version software is used for simulating each block of DDC at system level testing and Chip Scope Pro Analyzer tool is used for board level testing. Vitex-5 FPGA with speed -2 is the hardware used for implementing the design.

Keywords: CIC with Decimation, DDC, DDS, FPGA, ADC.

I. INTRODUCTION

Digital Down Conversion is a technique that takes a band limited high sample rate digitized signal, mixes the signal to a lower frequency and reduces the sample rate while retaining all the information. A fundamental part of many communications systems is Digital Down Conversion (DDC). Digital radio receivers often have fast ADC converters to digitize the band limited RF signal generating high data rates; but in many cases, the signal of interest represents a small proportion of that bandwidth. To extract the band of interest at this high sample rate would require a prohibitively large filter. A DDC allows the frequency band of interest to be moved down the spectrum so the sample rate can be reduced, filter requirements and further processing on the signal of interest become more easily realizable. At present Digital communication is more popular. It is a process of transferring signals, in digital format i.e., as bits. A transmitter, channel and a receiver are the main blocks of a communication system as shown in Fig.1. The DDC presented in this paper is the key component of Receiver. The digital IF signal from ADC is given as input to DDC. The speed of the ADC depends on the band of interest as the Nyquist’s theory states that the signal should be sampled at a rate "at least double the bandwidth of interest".

A DDC allows the frequency band of interest to be moved down the spectrum to baseband signal near to 80mHz such that further processing on the signals become easier. A DDC consists of three subcomponents –a direct digital synthesizer (DDS) which generates a complex sinusoid at the intermediate frequency, a pair of multipliers (in quadrature’s) to convert from IF to baseband, and a pair of low pass filter and decimators.

Fig.1. Flow Chart of the Project.
The multipliers perform the down conversion function conversion by creating a difference signals at the IF minus DDS frequency. The low pass filter passes only the desired signal and perform ant I alias filtering prior to decimation. The most common choice is a FIR filter for larger down sampling ratios. A Verilog code is generated for the designed DDC architecture and it is simulated using a testbench. This code undergoes simulation in which a netlist is created. Then the netlist is implemented, and a program file is generated which is dumped into the FPGA.

II. OVERVIEW OF DDC

Digital Down Conversion is a technique that takes a band limited high sample rate digitized signal, mixes the signal to a lower frequency and reduces the sample rate while retaining all the information. A fundamental part of many communications systems is Digital Down Conversion (DDC). Digital radio receivers often have fast ADC converters to digitize the band limited RF signal generating high data rates; but in many cases, the signal of interest represents a small proportion of that bandwidth as shown in Fig.2. To extract the band of interest at this high sample rate would require a prohibitively large filter. A DDC allows the frequency band of interest to be moved down the spectrum so the sample rate can be reduced, filter requirements and further processing on the signal of interest become more easily realizable. A DDC consists of three subcomponents –a direct digital synthesizer (DDS) which generates a complex sinusoid at the intermediate frequency, a pair of multipliers (in quadrature’s) to convert from IF to baseband, and a pair of low pass filter and decimators. The multipliers perform the down conversion function conversion by creating a difference signals at the IF minus DDS frequency. the low pass filter passes only the desired signal and perform ant I alias filtering prior to decimation. The most common choice is a FIR filter for larger down sampling ratios. Here the DDC consists of five basic blocks

- Input signal (LFM)
- DDS (Direct Digital Synthesizer)
- Mixer
- CIC (Cascaded integrate comb) with decimation

A. LFM Signal

The Linear Frequency Modulation (LFM) pulse compression technique on a generic signal model. Pulse compression allows achieving the performance of a shorter pulse using a longer pulse and hence gain of a large spectral bandwidth. The pulse compression technique plays a very important role for designing a radar system as shown in Fig.3. A linear FM chirp has a linear time frequency description as its frequency varies linearly over the pulse duration of the signal. In case of LFM frequency increases (up chirp) or decreases (down chirp) linearly with time. Following figure shows the time frequency characteristics of the signal.

![Fig.3. Depicts the frequency vs characteristics of a linear FM chirp.](image)

The ideal linear FM signal $X(t)$, is given by

$$X(t) = \text{rect}(t/T)A\exp(j\pi\beta t^2)$$  \hspace{1cm} (1)

Where,
- $A$=amplitude
- $T$=pulse width
- $t$ = time variable in sec
- $\beta$=LFM rate or chirp in hertz per sec.

The phase of the LFM signal is given by argument of the exponential expressed in radians

$$\Phi(t) = \pi\beta t^2$$  \hspace{1cm} (2)

A SAR receiver can beneficiate this property by using pulse matched filter to pass rejected noise and other signals, the ratio of the transmitted pulse duration to duration of the compressed pulse, known as pulse compression ratio, is equal to Bandwidth fig.4 shown as uncompressed LFM signal

![Fig.4. Uncompressed Linear frequency model.](image)

B. DDS (Direct Digital Synthesizer)

Direct digital synthesis (DDS) is a method of producing an analog waveform-usually a sine wave-by generating a time-
FPGA Implementation of Digital Down Converter

2^N = Length of the phase accumulator, in bits
F_{clk} = Internal reference clock frequency (system clock)

Changes to the value of M in the DDS architecture result in immediate and phase-continuous changes in the output frequency as shown in Fig.7. In practical application, the M value, or frequency tuning word, is loaded into an internal serial or byte-loaded register which precedes the parallel-output delta phase register. This is generally done to minimize the package pin count of the DDS device.

C. Mixer

A mixer, or frequency mixer, is a nonlinear electrical circuit that creates new frequencies from two signals applied to it. In its most common application, two signals at frequencies f_1 and f_2 are applied to a mixer, and it produces new signals at the sum f_1 + f_2 and difference f_1 – f_2 of the original frequencies, called heterodynes. Heterodyning is a radio signal processing technique invented in 1901 by Canadian inventor-engineer Reginald Fessenden that creates new frequencies by combining or mixing two frequencies. Heterodyning is used to shift one frequency range into another, new one, and is also involved in the processes of modulation and demodulation. The two frequencies are varying signal in digital form and then performing a digital-to-analog conversion. Because operations within a DDS device are primarily digital, it can offer fast switching between output frequencies, fine frequency resolution, and operation over a broad spectrum of frequencies. With advances in design and process technology, today’s DDS devices are very compact and draw little power. The ability to accurately produce and control waveforms of various frequencies and profiles has become a key requirement common to a few industries. Whether providing agile sources of low phase-noise variable frequencies with good spurious performance for communications, or simply generating a frequency stimulus in industrial or biomedical test equipment applications, convenience, compactness, and low cost are important design considerations.

Fig.5. DDS Block Diagram.

Continuous-time sinusoidal signals have a repetitive angular phase range of 0 to 2π. The digital implementation is no different. The counter’s carry function allows the phase accumulator to act as a phase wheel in the DDS implementation. To understand this basic function, visualize the sine-wave oscillation as a vector rotating around a phase circle (see Fig.5). Each designated point on the phase wheel corresponds to the equivalent point on a cycle of a sine wave. As the vector rotates around the wheel, visualize that the sine of the angle generates a corresponding output sine wave. One revolution of the vector around the phase wheel, at a constant speed, results in one complete cycle of the output sine wave. The phase accumulator provides the equally spaced angular values accompanying the vector’s linear rotation around the phase wheel as shown in Fig.6. The contents of the phase accumulator correspond to the points on the cycle of the output sine wave. Most DDS architectures exploit the symmetrical nature of a sine wave and utilize mapping logic to synthesize a complete sine wave cycle from ¼ cycle of data from the phase accumulator. The phase-to-amplitude lookup table generates all the necessary data by reading forward then back through the lookup table.

The relationship of the phase accumulator and delta phase accumulator form the basic tuning equation for DDS architecture:

\[ F_{out} = \frac{M}{2^N} \cdot F_{clk} \]  

\[ F_{out} = Output \ frequency \ of \ the \ DDS \]  

\[ M = Binary \ tuning \ word \]  

Fig.6. Digital Phase Wheel.

Fig.7. Signal flow through DDS Architecture.
combined in a nonlinear signal-processing device such as a vacuum tube, transistor, or diode, usually called a mixer. Mixers are widely used to shift signals from one frequency range to another, a process known as heterodyning, for convenience in transmission or further signal processing.

- In-Phase Signal
- Quadrature-Phase Signal

Fig.8.

This works on the (simplified) mathematical principle:

\[ \text{Frequency}(A) \times \text{Frequency}(B) = \text{Frequency}(A-B) + \text{Frequency}(A+B). \]

But aliases obtain at the mixer stage due to the difference frequencies which are removed in further stages using filtering techniques.

III. FILTERING TECHNIQUES

A. CIC (Cascaded Integrator–Comb)

A cascaded integrator–comb (CIC) is an optimized class of finite impulse response (FIR) filter combined with an interpolator or decimator. The two basic building blocks of a CIC filter are an integrator and a comb. An integrator is simply a single-pole IIR filter with a unity feedback coefficient:

\[ Y[n] = y[n-1] + x[n] \]  

(4)

This system is also known as an accumulator. The transfer function for an integrator on the z-plane is

\[ H_c(z) = \frac{1}{(1 - z^{-1})} \]  

(5)

Using the equations for a single pole system, we can determine that

\[ |H_e(e^{j\omega})|^2 = \frac{1}{2(1 - \cos \omega)} \]  

(6)

\[ \text{ARG}[H_e(e^{j\omega})] = -\tan^{-1}\left[\frac{\sin \omega}{1 - \cos \omega}\right] \]  

(7)

\[ \text{grd}[H_e(e^{j\omega})] = \begin{cases} \text{undefined} & \omega = 0 \\ \frac{1}{2} & \omega = 0 \end{cases} \]  

(8)

The power response is basically a low-pass filter with a −20 dB per decade (−6 dB per octave) roll off, but with infinite gain at DC. This is due to the single pole at z = 1; the output can grow without bound for a bounded input. In other words, a single integrator by itself is unstable.

Fig.9.

**Basic Integrator**: A comb filter running at the high sampling rate, \( f_s \), for a rate change of R is an odds metric FIR filter described by

\[ y[n] = x[n] - x[n - RM] \]  

(9)

In this equation, M is a design parameter and is called the differential delay. M can be any positive integer, but it is usually limited to 1 or 2. The corresponding transfer at \( f_s \).

\[ H_c(z) = 1 - z^{-RM} \]  

(10)

Again, we can determine that

\[ |H_c(e^{j\omega})|^2 = 2(1 - \cos R M \omega) \]  

(11)

\[ \text{ARG}[H_c(e^{j\omega})] = -\frac{RM \omega}{2} \]  

(12)

\[ \text{grd}[H_c(e^{j\omega})] = \frac{RM}{2} \]  

(13)

When R = 1 and M = 1, the power response is a high-pass function with 20 dB per decade (6 dB per octave) gain (after all, it is the inverse of an integrator). When RM ≠1, then the power response takes on the familiar raised cosine form with RM cycles from 0 to 2π.

Fig.10. Basic Comb.

Fig.11. Three Stage Decimating CIC Filter.

Fig.12. Three Stage Interpolating CIC Filter.

B. Frequency Characteristics

The transfer function for a CIC filter at \( f_{180} \)

\[ H(z) = H_c^N(z)H_e^N(z) = \frac{(1 - z^{-RM})^N}{(1 - z^{-1})^N} \]  

(14)
The magnitude response at the output of the filter can be shown to be

\[ |H(f)| = \left| \frac{\sin(\pi Mf)}{\sin(\pi f/R)} \right|^N \]  \hspace{1cm} (16)

For CIC decimators, the gain \( G \) at the output of the final comb section is

\[ G = (RM)^N \]  \hspace{1cm} (17)

Assuming two’s complement arithmetic, we can use this result to calculate the number of bits required for the last comb due to bit growth. If \( B_{\text{in}} \) is the number of input bits, then the number of output bits, \( B_{\text{out}} \), is

\[ B_{\text{out}} = \lceil N \log_2(RM) + B_{\text{in}} \rceil \]  \hspace{1cm} (18)

For a CIC interpolator, the gain, \( G \), at the \( i \)th stage is

\[ G_i = \begin{cases} 2^i & i = 1, 2, \ldots, N \\ 2N-i(2^i/2) & i = N + 1, \ldots, 2N \\ \end{cases} \]  \hspace{1cm} (19)

As a result, the register width, \( w_i \), at the \( i \)th stage is

\[ w_i = \lceil B_{\text{in}} + \log_2(G_i) \rceil \]  \hspace{1cm} (20)

And

\[ w_N = B_{\text{in}} + N - 1 \]  \hspace{1cm} (21)

If \( M = 1 \), rounding or truncation cannot be used in CIC interpolators, except for the result, because the small errors introduced by rounding or truncation can grow without bound in the integrator sections. It is now worth revisiting the unstable aspect of the integrator stages. It turns out that it is not a problem. For decimators, integrator overflow is not a problem if two’s complement math is used, and we don’t expect an overall system gain >1. For interpolators, the comb stages and zero stuffing will prevent integrator overflow.

IV. FPGA INTRODUCTION

A field programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing hence “field-programmable”. The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC). FPGAs can be used to implement any logical function that an ASIC could perform. They can be programmed one time or several times or dynamically. Field Programmable Gate Arrays (FPGAs) were first introduced almost two and a half decades ago. Since then they have seen a rapid growth and have become a popular implementation media for digital circuits. Contemporary FPGAs have large resources of logic gates and RAM blocks to implement complex digital computations. The advancement in process technology has greatly enhanced the logic capacity of FPGAs and has in turn made them a viable implementation alternative for larger and complex designs. Further, programmable nature of their logic and routing resources has a dramatic effect on the quality of final device’s area, speed, and power consumption.

A. Design Flow

The process of converting a circuit description into a format that can be loaded into an FPGA can be roughly divided into five distinct steps, namely: synthesis, technology mapping, mapping, placement and routing. The final output of FPGA CAD tools is a bit stream that configures the state of the memory bits in an FPGA. The state of these bits determines the logical function that the FPGA implements. Fig.13 shows a generalized software flow for programming an application circuit on an FPGA.

B. Implementation

This process includes a sequence of three steps

- Translation
- Mapping
- Placing and Routing

Bitstream Generation: A bit stream information is generated for the output NCD file which can be used to configure the target FPGA device. The bit stream contains information as to which SRAM bit of an FPGA is programmed to 0 or to 1. The bit stream generator reads the technology mapping, packing and placement information to program the SRAM bits of Look-Up Tables. The routing information of a DNCD file is used to correctly program the SRAM bits of connection boxes and switch boxes.

ML403 Board: In this project we use ML403 board of Virtex-4 FPGA family. The ML403 evaluation platform enables designers to investigate and experiment with features of the Virtex™-4 family of FPGAs. Powered by the XC4VFX12 device and supported by industry-standard peripherals, connectors and interfaces, the ML403 Virtex-4 FX Evaluation Platform offers a rich feature set that spans a wide range of applications as shown in Fig.14. It provides a comprehensive environment for developing embedded
designs based on the Virtex-4 FX FPGA. It supports multiple FPGA programming modes and interfaces. It is of low cost and supports a wide range of applications.

C. Features
- Virtex-4 FPGA: XC4VFX12-FF668-10.
- 64-MB DDR SDRAM, 32-bit interface running up to 266-MHz data rate.
- One 100-MHz clock oscillator (socketed) plus one extra open 3.3V clock oscillator socket.
- Stereo AC97 audio codec with line-in, line-out, 50-mW headphone, and microphone-in (mono) jacks.
- RS-232 serial port.
- 16-character x 2-line LCD display.
- One 4-Kb IIC EEPROM.
- VGA output: 140 MHz / 15-bit video DAC.
- PS/2 mouse and keyboard connectors.
- ZBT synchronous SRAM: 8 Mb on 32-bit data bus with no parity bits.
- Intel Strata Flash (or compatible) linear flash chips (8MB) 10/100/1000 tri-speed Ethernet PHY transceiver.
- USB interface chip (Cypress CY7C67300) with host and peripheral ports.
- Xilinx XC95144XL CPLD to allow linear flash chips to be used for FPGA configuration.
- Xilinx XCF32P Platform Flash configuration storage device.
- JTAG configuration port for use with Parallel Cable III or Parallel Cable IV cable.
- Onboard power supplies for all necessary voltages 5V @ 3A AC adapterPower indicator LED.

V. SIMULATION AND RESULTS
Simulation results of this paper is as shown in below Figs.15 to 23.
FPGA Implementation of Digital Down Converter

Fig.18. RTL Schematic of LFM.

Fig.19. LFM Signal 80mhz.

Fig.20. Block diagram of DDC.

Fig.21. RTL Schematic of DDC.

Fig.22. I-Channel output of DDC.

Fig.23. Q-Channel Output of DDC.

VI. CONCLUSION

Thus, a configurable Digital down Converter for Baseband signal has been developed. All the blocks in the DDC are efficiently designed using Xilinx and implemented on FPGA. This project can also be applicable for Narrowband of signals. The implementation of variable decimation to extract the actual signal from the band of signals received makes the design more important. The fulfilment of the speed requirements stated has been shown through the timing summary. The components are being designed such that the end users can customize the design according to their requirements by simply modifying certain parameters in each block. Also, as FPGA is chosen as the target technology, it results in a design with low power consumption, accurate performance, high integration and customizability.

VII. REFERENCES