Low Voltage Low Power Design of Self Boosting 3T Gain Cell for Embedded DRAM Applications

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Abstract: Embedded DRAM (eDRAM) due to its small cell size and non-radioed circuit operation has long been considered an alternative for replacing SRAM. However, conventional 1T/1C eDRAM limits voltage scaling and requires frequent power consuming refresh operations. A partial resolution to this problem is provided by Gain Cell (GC) eDRAM which exhibits high potential for low power consumption, high chip density, two port functionality and reduced refresh operations. Nonetheless, the gain cell do not provide full swing voltage levels due to these reduced refresh rates which requires boosted control signals to restore the voltage swing using an additional power supply or a charge pump. In this paper, we present a self-boosting 3T gain cell eDRAM operating on a single supply voltage and compare its performance to 2T gain cell eDRAM and 6T SRAM on a 0.25µm CMOS technology operating on 1.1 V.

Keywords: eDRAM, Gain Cell, Low Power Consumption.

I. INTRODUCTION

The modern-day chip designers encounter stringent power specifications to optimize the overall power consumption. Concurrently, the demand for more features and enhanced performance continues to increase, but at the liability of power with the circuit design adapting to newer technologies, exhibiting more stricter power constraints due to increase in chip density, operating speed and circuit complexity. One of the aspects that has crucially contributed to such advancements is memories that have occupied large portions of chip. It is prominently due to the large 6 – transistor SRAM cell and its area consuming peripheral circuitry. This has fetched immense attention to the compact high-density chip design enduring to the revolutionary changes encountered in the new era of processing technology.

II. STATIC RANDOM ACCESS MEMORY

A memory circuit refers to as static if it preserves the stored data for an indefinite amount of time, without any periodic refresh operation. Static RAM cell comprise of two inverters latched to each other with NMOS access transistors coupled between differential bit lines. These access transistors are activated by word line assertion for read or write operations. Conventionally, 6T SRAM due to its refresh free operation, longer data retention and high access speed, has always been the classic choice for the implementation of embedded memories. However, the increment in the memory capacities i.e., number of bits per die area (chip density) has significantly replaced larger SRAM cell with smaller alternatives. High memory bandwidth can be achieved by simultaneous write and read access to the memory cell. But this dual port functionality for SRAM requires more number of transistors demanding for larger die area as shown in Fig.1. One of the major issues encountered in SRAM cell is off transistor leakage current causing stand by static power consumption. To overcome the dynamic power concerns, voltage scaling has been considered one of the most effective solutions. However, this would cause impeded functionality of the memory cell on lowering supply voltage, which is undesired. Hence, an appropriate alternative fabricated by standard processes, with low operating voltage, high chip density, longer data retention time and low power consumption is required in replacement of an SRAM cell.

Fig. 1. 6T SRAM Cell.
III. GAIN CELL EMBEDDED DRAM

A. Embedded DRAM (eDRAM)

An eDRAM is a dynamic random-access memory (DRAM) integrated on the same die along with other ICs. An eDRAM costs higher per bit compared to external DRAM chips. Although the advantage of the performance of eDRAM balances its disadvantage of cost over the stand-alone DRAM cell.

B. Gain Cell

Gain cells are dynamic memory bit cells consisting of two to three transistors and optional MOSCAP or diode. The additional optional devices, when compared to their 1T DRAM counterparts, are used to both increase the in-cell storage capacitance and also to amplify the readout charge flow as compared to the stored charge level. Hence, the name “gain” cells. Gain cells provide higher bit cell density on a chip due to the reduced number of components in the bit cell compared to the standard SRAM bit cell. It provides two port functionality reducing dynamic power consumption. Since the number of components in the have considerably been lowered, therefore, the leakage power has reduced significantly. In spite of these advantages, gain cell suffers from several limitations, one of which is small internal storage capacitor. This leads to shorter data retention times which require periodical power-hungry refresh operations.

C. 2T Gain Cell

The 2T gain cell eDRAM consists of two transistors: one PMOS and one NMOS transistor. To write or read the data from the cell, the entire cell need not be used. For write operation, only the write transistor of the cell is activated whereas the read transistor is deactivated as shown in Fig.2. Similarly, for read operation, only the read transistor of the cell is activated whereas the write transistor is deactivated. This partial activation of the cell reduces the power consumption. The 2T gain cell has separate bit lines and separate word lines for write and read operations. The bit lines are used to write or read data from the cell whereas the word lines are used to gain access to the cell. Before every read and write operations, the bit lines have to be pre-charged to Vdd. Despite providing considerable advantages over SRAM, 2T Gain Cell have certain limitations like it requires periodic refresh operations, does not provide full swing ‘0’, charge injection and clock feed – through cause voltage step at storage node.

IV. 3T GAIN CELL

To reduce the frequency of periodic refresh operations of 2T gain cell implementations, boosted control signals are required to write full swing voltage levels. This boost is either acquired from an extra power supply or an on-chip charge pump which causes a substantial overhead in the silicon die area as shown in Fig.3. Furthermore, degradation of stored logic levels is caused by charge injection and clock feed – through which results in an erroneous output. These drawbacks can be overcome by appending an NMOS transistor in parallel to the PMOS write transistor in 2T gain cell, resulting in a 3T Gain cell. The write transistors have complementary word lines.

Fig. 3. 3T Gain Cell EDRAM.

A. Cell Operation

3T gain cell has three modes of operation depending on the word line assertions.
- Write Mode (WWLp = 0, WWLn = 1, RWL = 1)
- Read Mode (WWLp = 1, WWLn = 0, RWL = 0)
- Stand – by Mode (WWLp = 1, WWLn = 0, RWL = 1)

The bit lines are used to write or read data from the cell whereas the word lines are used to gain access to the cell. Before every read and write operations, the bit lines have to be pre-charged to Vdd.

Write ‘0’ Operation: Writing data into a memory cell indicates modification of contents of the cell. Let us assume the storage node SN previously stored ‘1’. Due to pre-charge cycle, both bit lines WBL and RBL are logic high. To write ‘0’, the write bit line WBL has to be pulled down to ground. To perform write operation, write word line is asserted i.e., WWLp = 0 and WWLn = 1 which turns write transistors PWT and NWT on.

This provides a low resistance path for the storage node to discharge to ground making its final logic level to ‘0’. Hence ‘0’ has been written in the gain cell. During write operation read word line RWL should be ‘1’ so that there is no potential difference between RBL and RWL as shown in Fig.4.
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Fig. 4. 3T Gain Cell Write ‘0’ Operation.

Read ‘0’ Operation: To read ‘0’ from the cell means that storage node SN = 0. During read operation, the read word line RWL is made ‘0’. As SN = 0, read transistor RT does not turn on which provides a high resistance path between its drain and source terminals. Therefore no current passes through the read transistor. As RBL retains its pre-charged logic value ‘1’, it is read as ‘0’ by sense inverter in read circuitry as shown in Fig.5.

Fig. 5. 3T Gain Cell Read ‘0’ Operation.

Write ‘1’ Operation:

Let us assume the storage node SN previously stored ‘0’. Due to pre-charge cycle, both bit lines WBL and RBL are logic high. To write ‘1’, the write bit line WBL retains its pre-charged logic ‘1’. To perform write operation, write word line is asserted i.e., WWLp = 0 and WWLn = 1 which turns write transistors PWT and NWT on as shown in Fig.6. This provides a low resistance path for the storage node to charge to ‘1’. Hence ‘1’ has been written in the gain cell. During write operation read word line RWL should be ‘1’ so that there is no potential difference between RBL and RWL.

Read ‘1’ Operation: To read ‘1’ from the cell means that storage node SN = 1. During read operation, the read word line RWL is made ‘0’. As SN = 1, read transistor RT turns on which provides a low resistance path for RBL to discharge from ‘1’ to ‘0’. This is read as ‘1’ by sense inverter in read circuitry as shown in Fig.7.

Fig. 7. 3T Gain Cell Read ‘1’ Operation.

Stand – by Mode:

In stand-by mode, both write and read word lines are deactivated. As WWLp = 1 and WWLn = 0, the write transistors PWT and NWT are turned off. Hence no data can be written into the cell as shown in Fig.8. Therefore, the cell holds the data that was previously written in the cell. If the storage node is logic ‘1’ then read transistor RT turns on. As there is no potential difference between the source and drain terminal, the read bit line retains its pre-charged value. If the storage node is logic ‘0’ then read transistor RT is off. The read bit line retains its pre-charged value as shown in Fig.9.

Fig. 8. 3T Gain Cell Stand – by Mode when ‘0’ is stored.

Fig. 9. 3T Gain Cell Stand – by mode when ‘1’ is stored.
A write operation is performed by discharging a pre-charged write bit line to ground or retaining the pre-charged logic level of the other bit line depending on the input data that is to be written in the memory cell as shown in Fig.10. Discharging of the write bit line is performed by providing a low resistance – conducting path from write bit line to ground. Retaining the bit line charge is performed by providing a high resistance – non conducting path from write bit line to ground. This task is accomplished using a write circuitry coupled with a bit line driver circuitry.

The write operation on a memory cell takes place only when the column in which the memory cell is present in a memory array is selected. This is selected using the column_select signal which is the column decoder output.

A read operation is performed when the read word line is asserted i.e., RWL = 0. The status of the read bit line depends on the logic level stored in the cell as shown in Fig.11. The logic state of RBL is inverted to determine the data stored in the cell. If the pre-charge RBL is discharged, then it is inverted to read the data stored in the cell as ‘1’. If RBL retains its pre-charged value then it is inverted to read as ‘0’. If RWL=1 then Read driver transistor RDT is off which does not let any RBL logic state to be passed on to the inverter making the read circuitry to present previous logic state as its output at data_out.
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D. 1 – bit 3T Gain Cell with Read – Write Peripherals

V. SIMULATION RESULTS

Simulation results of this paper is as shown in bellow Figs.13 and 14.

VI. POWER ANALYSIS

Average Power Consumption and the number of transistors used in the design of 6T SRAM, 2T eDRAM and 3T eDRAM bit cell have been compared and also along with the peripheral circuitry at 1.1 V for 0.25μm CMOS technology as shown in Figs.15 to 18.

TABLE V: Comparison of Average Power Consumption

<table>
<thead>
<tr>
<th>Architecture</th>
<th>6T SRAM</th>
<th>2T eDRAM</th>
<th>3T eDRAM</th>
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</thead>
<tbody>
<tr>
<td>1 – bit Cell</td>
<td>1.5529 μW</td>
<td>0.1369 μW</td>
<td>0.1230 μW</td>
</tr>
<tr>
<td>1 – bit Cell with Peripherals</td>
<td>65.4541 μW</td>
<td>24.96 μW</td>
<td>25.4580 μW</td>
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</tbody>
</table>

TABLE VI: Comparison of Total Number of Transistors

<table>
<thead>
<tr>
<th>Architecture</th>
<th>6T SRAM</th>
<th>2T eDRAM</th>
<th>3T eDRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 – bit Cell</td>
<td>6</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>1 – bit Cell with Peripherals</td>
<td>66</td>
<td>27</td>
<td>30</td>
</tr>
</tbody>
</table>
VII. CONCLUSION

In this paper, it has been observed that average power consumed by 3T 1-bit Gain Cell eDRAM is less compared to that of 2T eDRAM and 6T SRAM. However the 3T gain cell with peripheral circuits consumes more power than 2T gain cell but less than 6T gain cell. Moreover, the number of transistors of 2T gain cell is less than both 3T gain cell and 6T SRAM. But 3T gain cell overcomes the charge injection and clock feed-through effects on the memory cell compared to 2T gain cell, gives full swing voltage levels and has less power consumption compared to 6T SRAM. Therefore 3T gain cell eDRAM is preferred over 6T SRAM and 2T gain cell eDRAM.

VIII. REFERENCES


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