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Realization of Logic Functions using Reversible Logic Gates

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Abstract: In recent years, reversible logic has emerged as a promising computing paradigm having application in low power CMOS circuits, Quantum Computing, Nanotechnology, and Optical Computing. In this paper, the authors have realized logic functions using only one Reversible gate, Fredkin gate. The logic gates has 2 inputs and can realize various logic functions. In order to demonstrate the design of logic functions, a Fredkin gate used as a 2- input multiplexer and a 4- input multiplexer is designed using 2 to 1 multiplexers. Furthermore different combinations of inputs are used to realize the different logic functions through it.

Keywords: Reversible Logic, Fredkin Gate, Multiplexer, Low Power CMOS Circuit.

I. INTRODUCTION

Researchers like Landauer have shown that for irreversible logic computations, each bit of information lost generates kTln2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed [1]. Bennett showed that kT ln2 energy dissipation would not occur, if a computation is carried out in a reversible way [2], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible circuits are those circuits that do not lose information. The reversible logic operations do not erase (lose) information and dissipate very less heat. Thus, reversible logic is likely to be in demand in high speed power circuits. Reversible circuits are of high interest in low-power CMOS design [7], optical computing [8], quantum computing [9] and nanotechnology [10]. The most prominent application of reversible logic lies in quantum computers. A quantum computer can be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates. Reversible computation in a system can be performed only when the system comprises of reversible gates. These gates can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between input and output vectors. Thus, an NXN reversible gate can be represented as

$$Iv= (I1,I2,I3,I4,\ldots\ldots\ldots\ldots\ldots\ldots IN) \quad (1)$$

$$Ov= (O1,O2,O3,\ldots\ldots\ldots\ldots\ldots\ldots OP) \quad (2)$$

Where Iv and Ov represent the input and output vectors respectively. Conventional logic gates are irreversible since input vector states cannot be uniquely reconstructed from the output vector states. There are a number of existing reversible gates such as Fredkin gate[3,4,5], Toffoli Gate (TG) [3, 4] Thus, the proposed design is designed in an optimal manner by choosing the reversible Fredkin[3,4,5] gate. Also in the synthesis of reversible circuits direct fan-out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits.

- The number of Reversible gates (N): The number of reversible gates used in circuit.
- The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility. .
- Gate levels (GL): This refers to the number of levels in the circuit which are required to realize the given logic functions

This paper is organized as follows: Section II gives the brief introduction of the reversible logic gates and gates required for the present work. In Section III, the design of multiplexers with Fredkin gate is demonstrated. Section IV describes the Logic function block and its implementation. The simulation and Synthesis results are shown in section IV. Finally, Section V concludes with scope for further research

II. BASIC REVERSIBLE GATES

A. There are a Number of Existing Reversible Gates in the Literature.

Some of the basic reversible logic gates are,

1. Feynman gate: Fig.1 shows a 2x2 Feynman gate [6]. The input vector is I (A, B) and the output vector is O (P, Q) and the relation between input and output is given by

$$P=A,\ Q = A \oplus B. \quad (3)$$

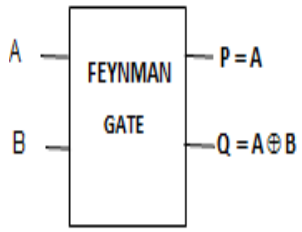

Fig.1. Feynman Gate.

2. Double Feynman gate (F2G): Fig. 2 shows a 3x3 Double Feynman gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R) and output is defined by

$$P = A, Q = A \oplus B, R = A \oplus C \quad (4)$$

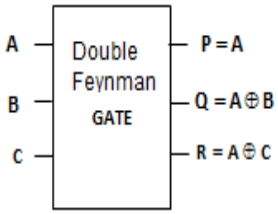

Fig.2.Double Feynman Gate

3. Fredkin Gate: Fig 3 shows a 3*3 Fredkin gate [4]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by

$$P=A, Q=A'B \oplus AC \text{ and } R=A'C \oplus AB \quad (5)$$

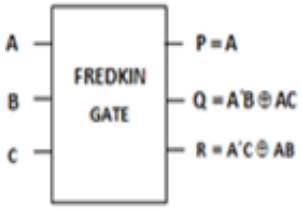

Fig.3. Fredkin Gate

4. Peres Gate: Fig 4 shows a 3*3 Peres gate [11]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by

$$P = A, Q = A \oplus B \text{ and } R=AB \oplus C \quad (6)$$

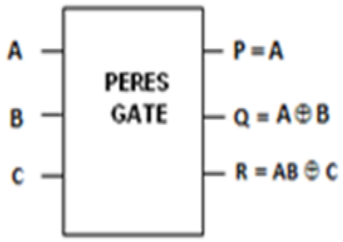

Fig.4. Peres Gate.

III. PROPOSED WORK

There are many existing designs to demonstrate the Logic functions. In these combinations of different reversible gates are used to realize those functions. In this paper authors have used only one type of reversible gate, Fredkin gate for realizing multiplexer and logic function block.

A. Fredkin Gtae used as 2 to 1 Multiplexer

Initially Fredkin gate is used as 2 to 1 multiplexer which is shown in Fig 5. This is demonstrated using one fredkin gate. It has two garbage outputs, and zero constant inputs.

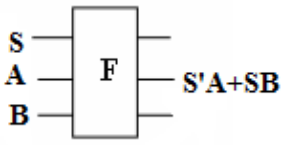

Fig.5. 2 to 1 Mux

Fig 5 shows 4 to 1 multiplexer using 2 to 1 multiplexers. This is realized using 3 fredkin gates. It has 6 garbage outputs, and zero constant inputs.

B. 4 to 1 Multiplexer

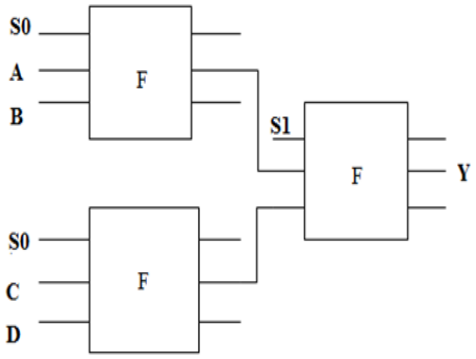

Fig.6. 4 to 1 Mux

C. Logic Functions

Fig 7 shows the block diagram of 4 to 1 multiplexer which is used as general logic function block. By giving various input combinations, different logic functions are obtained. Here mux is used as universal gate. Table 1 shows various logic functions.

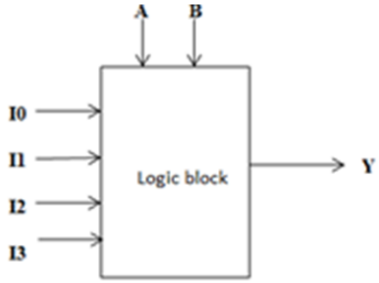

Fig.7. Logic Function Block.

TABLE I. Truth Table

I3	I2	I1	I0	Function
0	0	0	1	NOR
0	1	1	0	XOR
0	1	1	1	NAND
1	0	0	0	AND
1	1	1	0	OR
1	0	0	1	XNOR
0	0	1	1	NOT (A')
0	1	0	1	NOT (B')

TableII shows the comparison of the important parameters like number of gates, number of garbage outputs, number of gate levels and number of constant inputs of different implementations.

TABLE II. Comparison

Circuit	No.of Constant inputs	No.of Garbage outputs	No.of Reversible gates
2 :1 mux	0	2	1
4:1 mux	0	6	3
Logic function block	0	6	3

IV. SIMULATION AND SYNTHESIS RESULTS

The behavior of the 2 to 1 Mux, 4 to 1 Mux and Logic function block are verified using Xilinx ISE 14.1 and simulated using ISim. The simulated results are shown in figs 8-11. The Synthesis is performed using XILINX XST tool and is shown in fig 12 and 13.

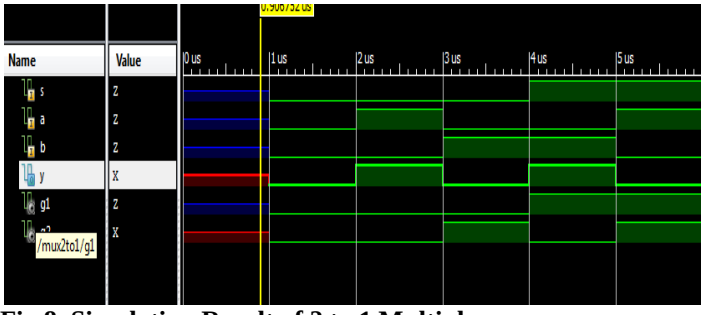

Fig.8. Simulation Result of 2 to 1 Multiplexer.

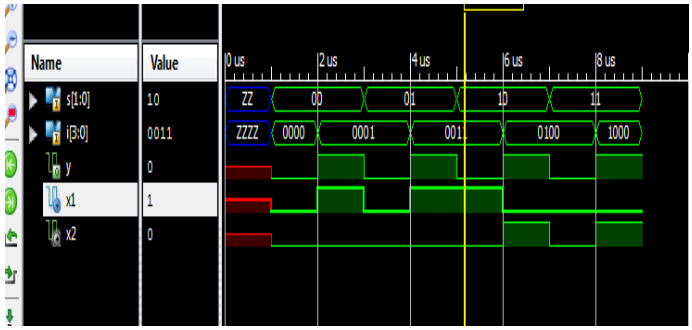

Fig.9. Simulation Result of 4 to 1 Multiplexer.

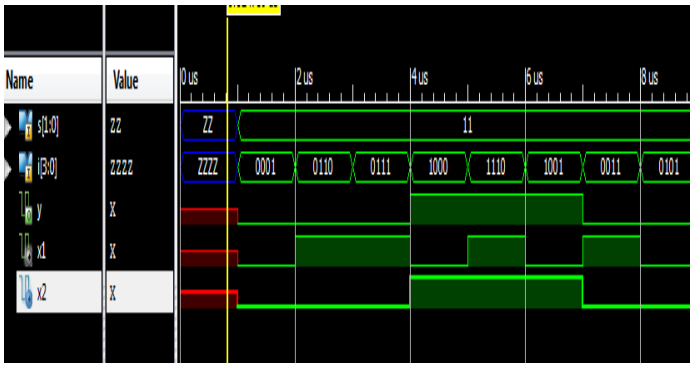

Fig.10. Simulation Result of Logic Block.

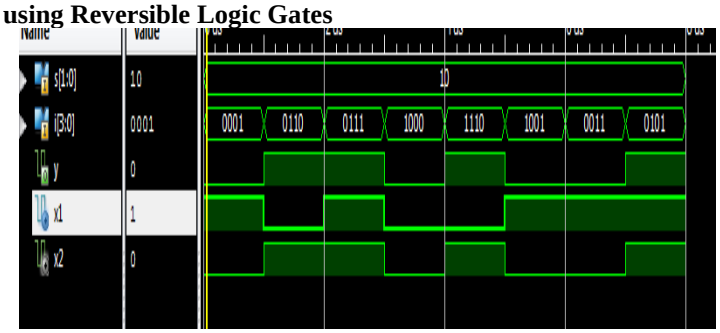

Fig.11. Simulation Result of Logic Block.

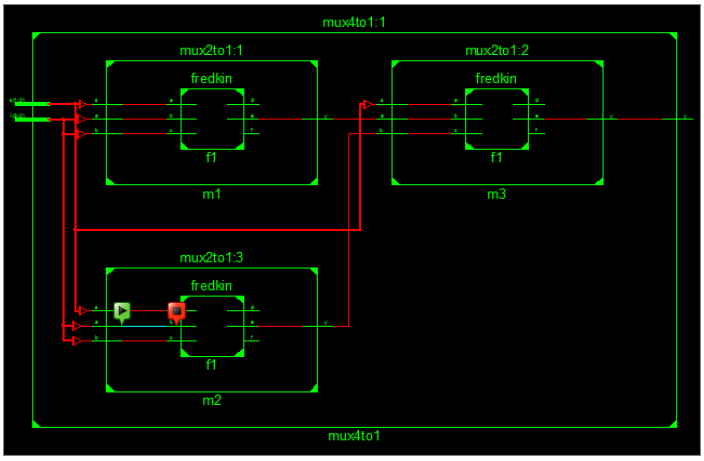

Fig.12. Synthesis of Logic Function Block.

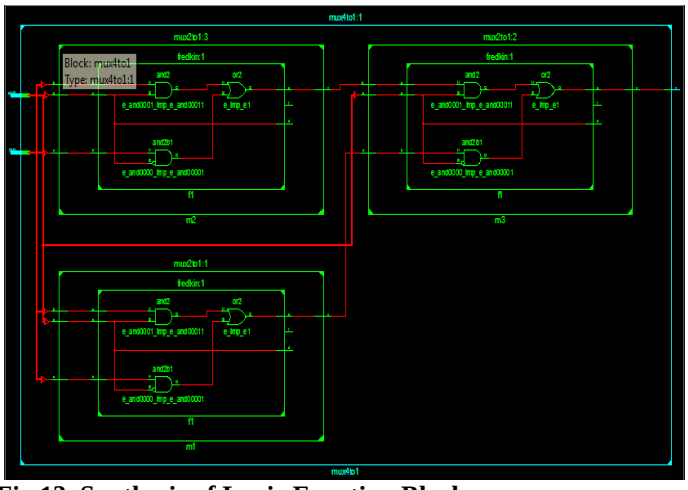

Fig.13. Synthesis of Logic Function Block

V. CONCLUSION

In this paper, the authors demonstrated only Fredkin gate as 2 to 1 mux, 4 to 1 mux and logic function block. The proposed circuit has less number of garbage outputs. These circuits are used in low power applications such as Quantum computers and Nanotechnology.

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