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GDI Techniques for Low Power Digital Circuits

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Abstract: The gate diffusion input (GDI) is a novel technique for low power digital circuits design. This technique reduces the power dissipation, propagation delay, area of digital circuits and it maintains low complexity of logic design. These limitations can be overcome by modified GDI and full swing GDI techniques. In this paper, basic building blocks of digital systems are analysed and comparisons are made based on complementary CMOS and GDI design techniques.

Keywords: Pass Transistors, Transmission Gate, CMOS, Gate Diffusion Input, Low Power Digital.

I. INTRODUCTION

Power management has become a major issue in the development of a digital system especially in the portable devices in which enhancement of the battery life time and reducing the charging time are becoming a challenging issue day by day. The major problem in the power management is power dissipation [1]. Technology scaling leads to increase leakage current which leads to increase in sub threshold leakage power therefore reduction of the leakage power nothing beet minimizing power dissipation [2]. There are different techniques existed. Gate diffusion input (GDI) technique is one to minimize the power dissipation. One form of logic that is popular in low power digital circuits is pass-transistor logic[3][4]. Formal methods for deriving pass transistor logic have been presented for nMOS. They are based on model, where a set of control signals is applied to the gates of n transistors[5]. Another set of data signals are applied to the sources of the n-transistors. However most of the Pass transistor logic implementations have two basic Techniques, First the threshold drop across the single channel pass transistors results in reduced current drive and hence slower operation at reduced power supply voltages; this is particularly important for low power design since it is desirable to operate at lowest possible voltage level Second, the high input voltage level[6][7]. In this paper, basic building blocks of digital systems are analysed and comparisons are made based on complementary CMOS and GDI design techniques.

II. TECHNICAL SURVEY

Tanner tool is a spice computer analysis programmed for analogue integrated circuits tanner EDA solutions by mentor graphics provides a complete line of EDA that drive innuation for the design. Layout and verification circuits (ICS).

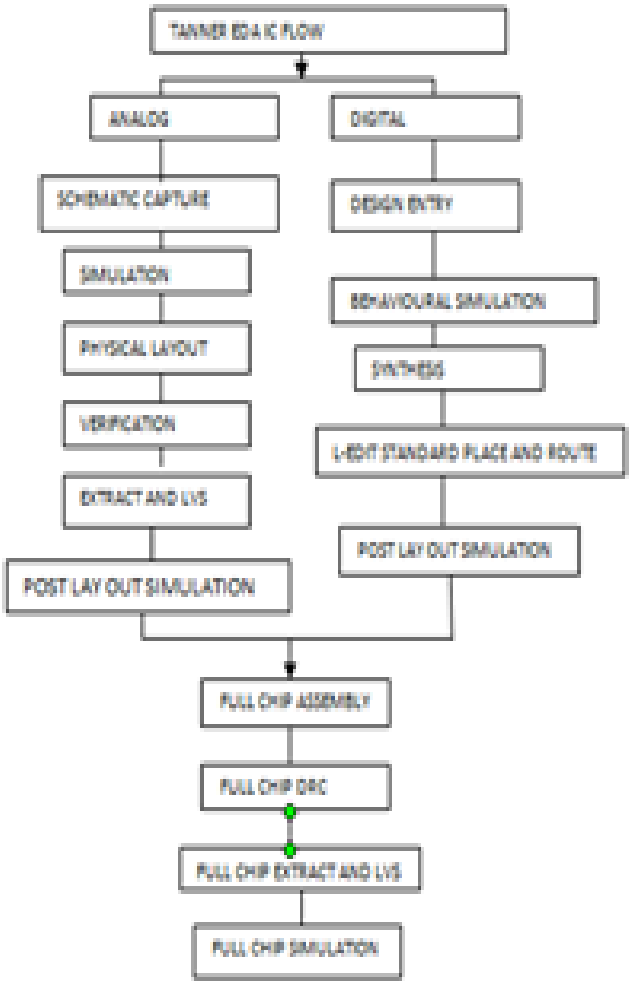

Fig 1. Flow diagram.

III. REVIEW ON CMOS AND GDI TECHNIQUES

Gate diffusion input (GDI) design technique was introduced as a promising alternative to complementary CMOS logic design. Originally proposed for fabrication in silicon on insulator (SOI) and twin-well CMOS process GDI methodology allow implementation of a wide range of complex logic functions using only two transistors. Pass Transistors, Transmission Gates and Gate Diffusion Input are different techniques low complexity of logic design inreduces the power dissipation, propagation delay, area of digital circuits. Even though CMOS logic design plays major role in designing

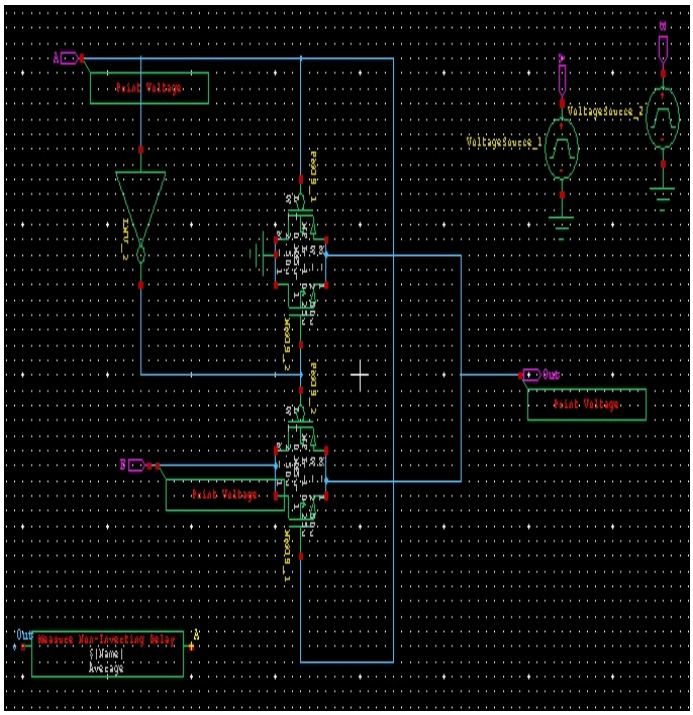

Fig 2. Schematic of AND Gate using Transmission gates.

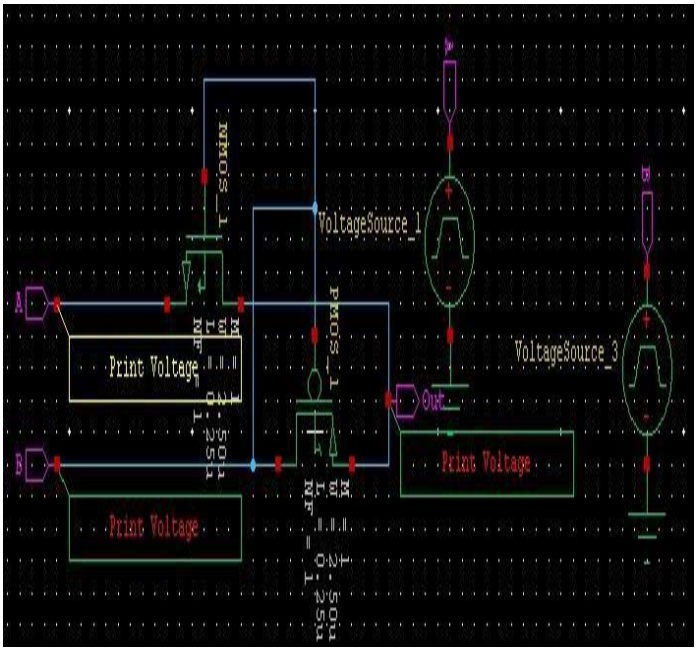

Fig 3. Schematic of AND Gate using Pass Transistors.

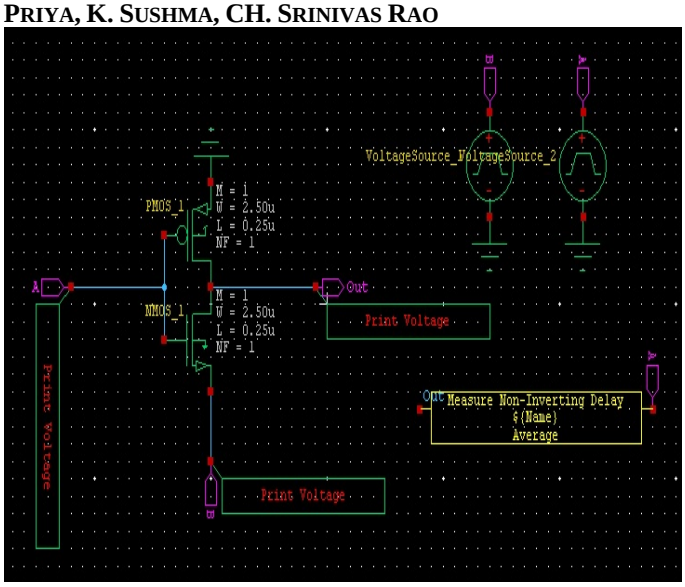

Fig 4. Schematic of AND Gate using GDI Logic.

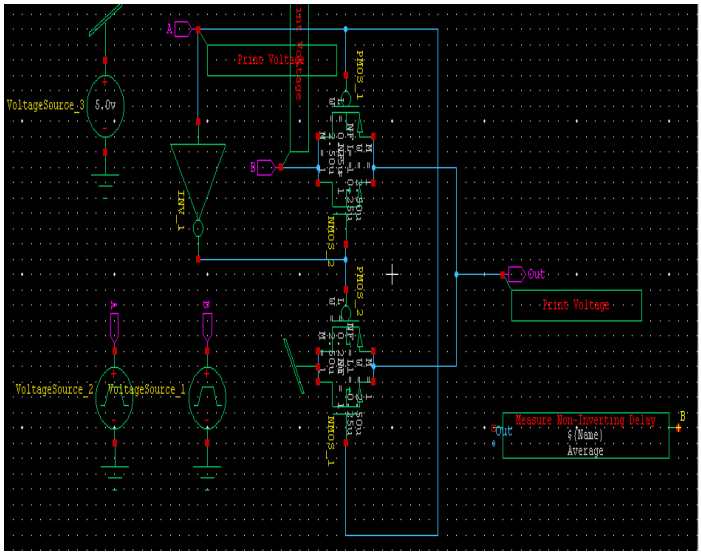

Fig5. Schematic of OR Gate using Transmission gates.

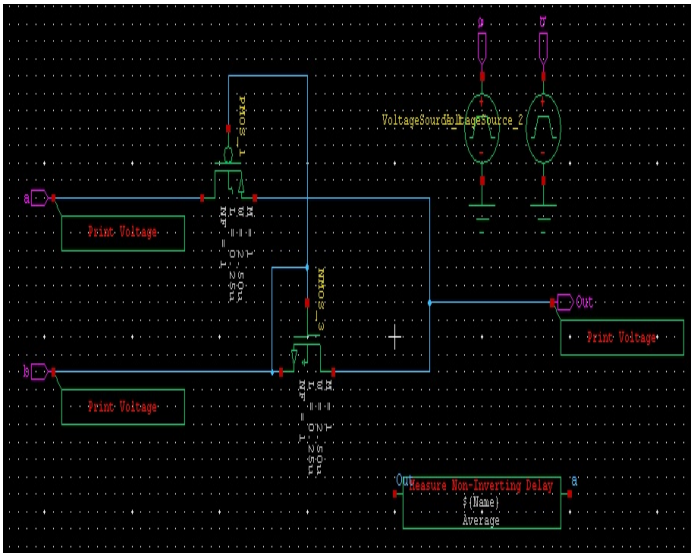

Fig 6. Schematic of OR Gate using Pass Transistors.

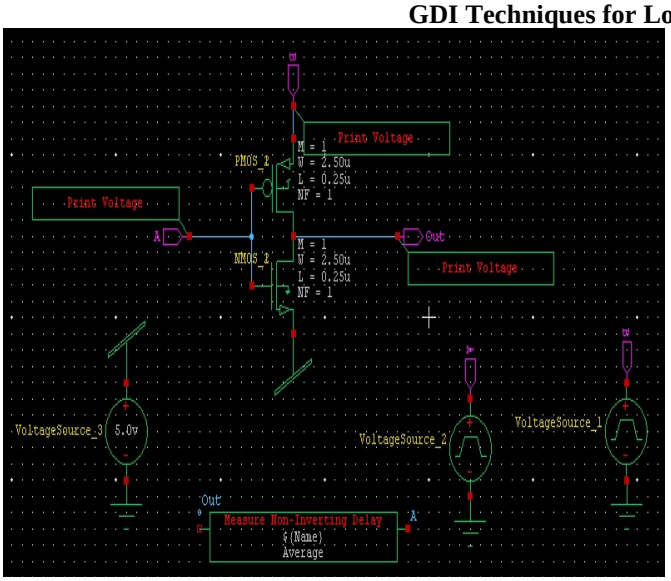

Fig 7. Schematic of OR Gate using GDI Logic.

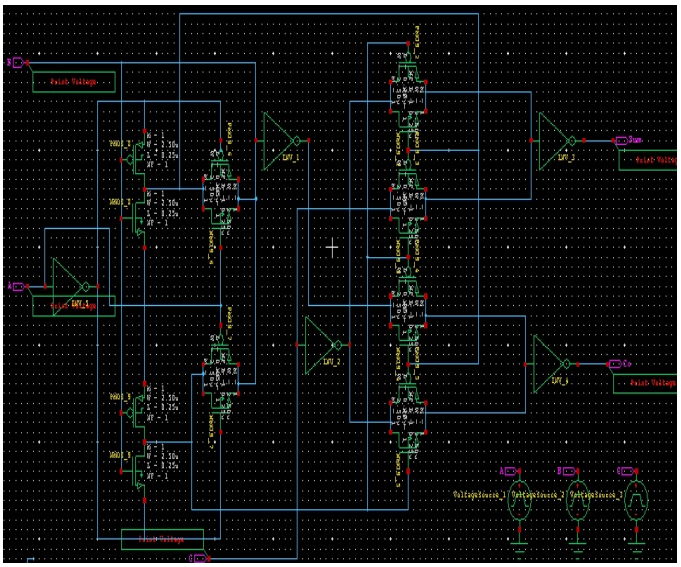

Fig8. Schematic of FULL ADDER using Transmission gates.

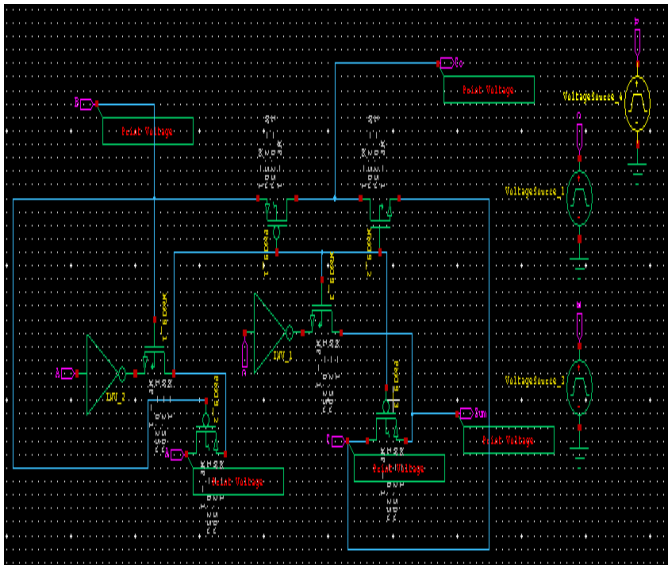

Fig 9. Schematic of FULLADDER using Pass Transistors.

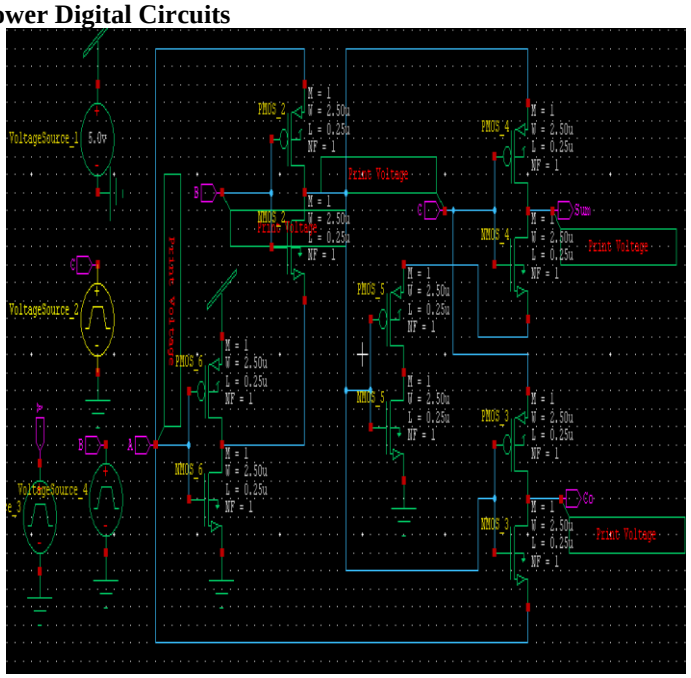

Fig10.Schematic of FULLADDER using Transmission gates.

devices with low power consumption, the switching activity of CMOS devices causes more power consumption Reduction of the power dissipation is obtained by reducing the capacitance in the circuit. The first step is to use minimum size transistors whenever possible. The second step is to use circuits, which heavily utilize transmission gates, and to implement these gates with single n-type transistors (Pass Transistor logic) instead of the two transistors generally used. Since the eliminated p- type transistor is usually larger than the n-type one, the input capacitance is reduced by a factor of more than 2. This reduction of input capacitance results in decrease in the delay of the circuit and reduction of the dynamic power dissipation. Gate Diffusion Input(GDI) design technique was introduced as a promising alternative to complementary CMOS Logic design. One of the common problems of pass transistor design methods is the low swing of output signals because of the threshold drop across the single channel pass transistors. In existing Pass transistor logic techniques additional buffering circuitry is used to overcome this problem. a high-speed and multipurpose logic style for low power electronics design, known as Gate Diffusion Input (GDI) with less power dissipation, reduced area, and efficient implementation of broad variety of logic functions. But this basic Gate Diffusion Input (GDI) logic style suffers from some practical limitations like swing degradation, fabrication complexity in standard CMOS process and bulk connections. These limitations can be overcome by modified gate diffusion input (Mod-GDI) logic style. This modified gate diffusion input (Mod-GDI) logic style allows reducing power consumption, delay and area of digital circuits.

VI. RESULTS AND DISSCUSSIONS

The circuits designed and simulated using Tanner EDA tools with S-EDIT,T-SPICE,W-EDIT. The obtained results are presented in this section. Generated plots for each circuit in SECTION III are mentioned in the following sub sections.

A. AND Gate

Fig 11. AND Gate output Waveforms.

B. OR Gate

Fig:12 corresponds to the generated plot for OR gate using Trasmission, Pass transistor, Gate Input Diffussion Techniques.

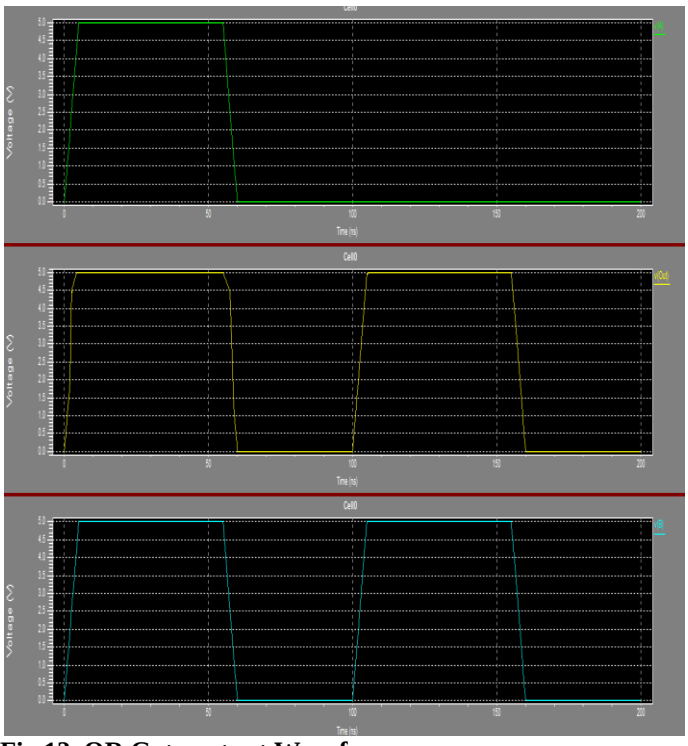

Fig 12. OR Gate output Waveforms.

C. Full Adder

Fig:13 corresponds to the generated plot for full adder using different Techniques.

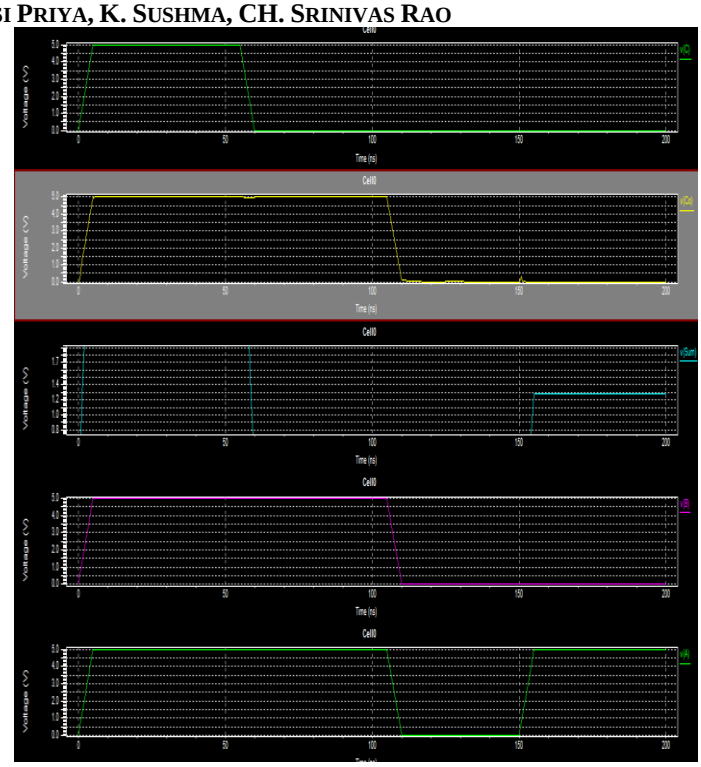

Fig 13. output Waveforms of FULL ADDER circuits.

VII. COMPARISON

A comparison study based on different techniques is tabulated in Table.1.It shows that the transistors used in all the techniques are equal and the power dissipation at 5v is less for OR gate using GDI technique and high for Full adder using transmission gate.

TABLE.1: COMPARISON

Type of logic	No.of transistors			Power dissipation at Vin=5V		
	AND	OR	FULL ADDER	AND	OR	FULL ADDER
Transmission	6	6	26	4.975	5.00	20.62
Pass transistor	2	2	10	4.036	4.036	12.90
Gate Diffusion Input	2	2	10	4.000	3.99	11.7

VIII. CONCLUSION

Hierarchical designs are in turn dependent up on the present proposed designs. Use of GDI further reduces the complexities at chip design level and provides best results in comparison with previous techniques. Sequential logic design with GDI is currently being explored as well as technology compatibility. Hierarchical designs are in turn dependent up on the present proposed designs. Use of GDI further reduces the complexities at chip design level and provides best results in comparison with previous techniques. Sequential logic design with GDI is currently being explored as well as technology compatibility

IX. REFERENCES

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